

Milgauss_TL

Schematics Document

DY : None Installed
SPIN3 : Yacht_TL
SPIN5 : Milgauss_TL

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Milgauss_TL

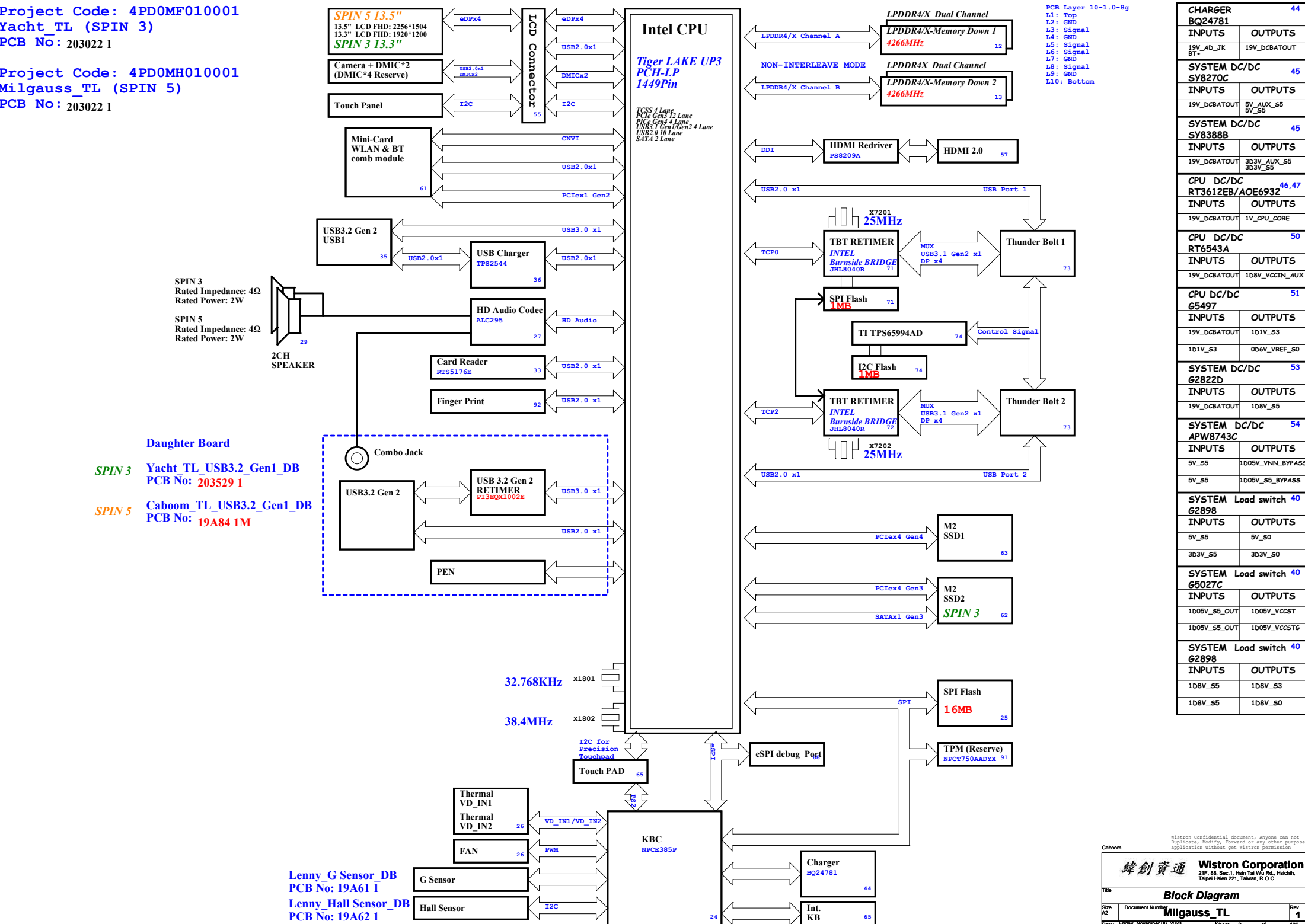
Rev
1

Date: Friday, November 06, 2020

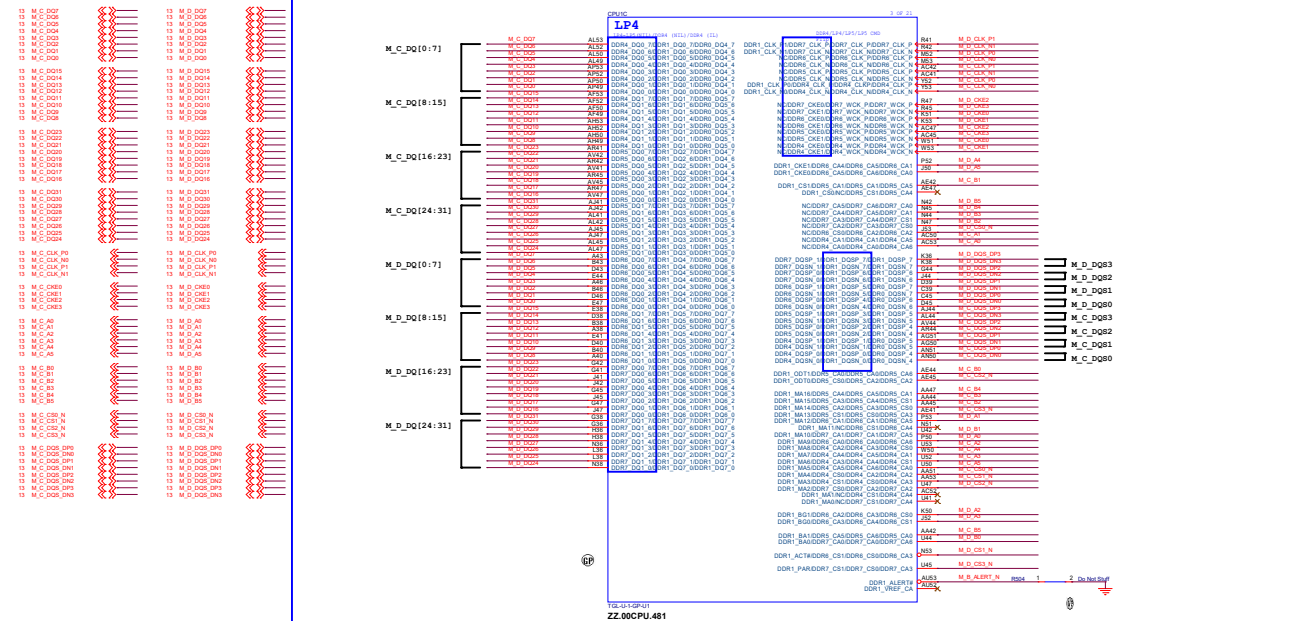
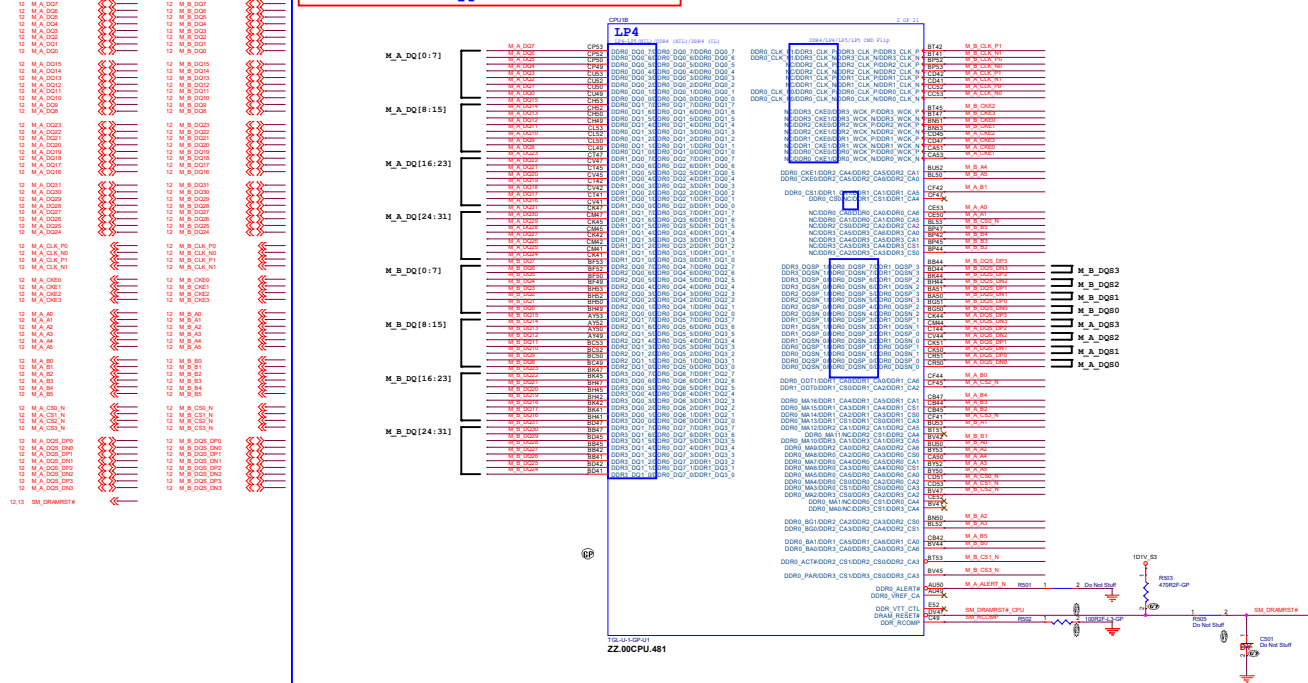
Sheet 1 of 106

Project Code: 4PD0MF010001
Yacht_TL (SPIN 3)
PCB No: 203022 1

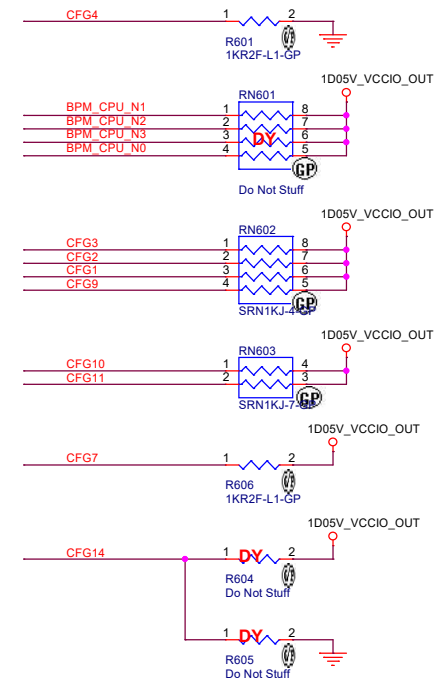
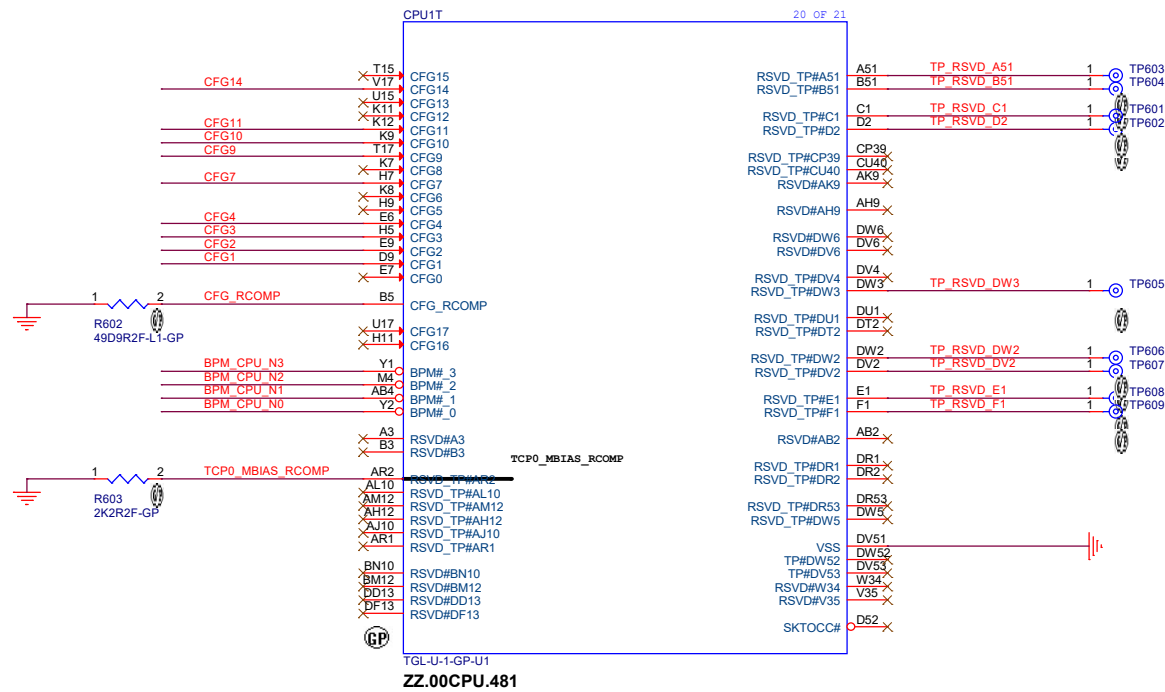
Project Code: 4PD0MH010001
Milgauss_TL (SPIN 5)
PCB No: 203022 1



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		1			



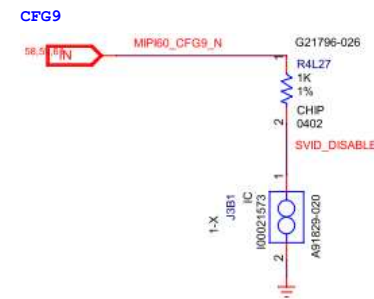
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Document Number: 607872 Ver 1.1

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

Document Number: 612304 Ver 1.0



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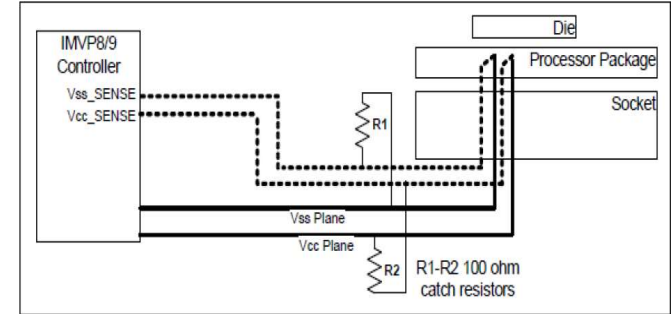
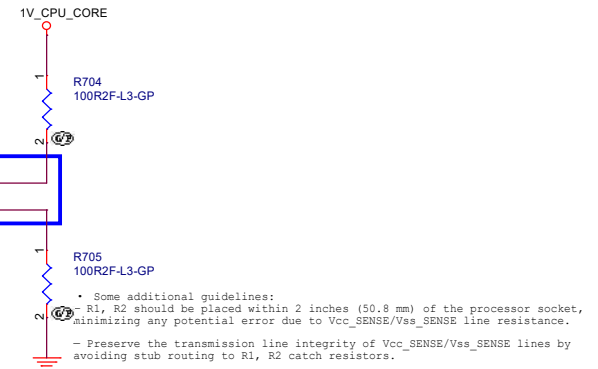
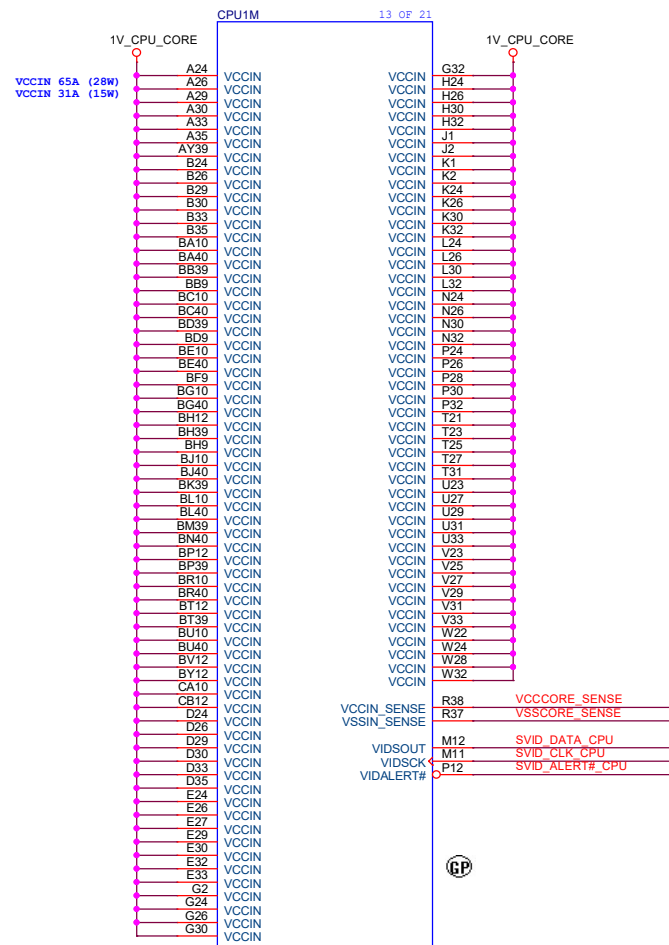
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Title CPU (CFG/ST)

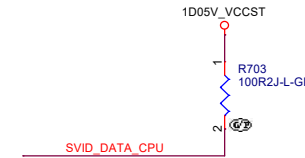
Size A3 Document Number Milgauss_TL Rev 1

Date: Friday, November 08, 2020 Sheet 6 of 106

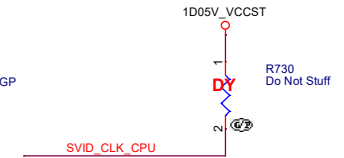
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU
46 VCCCORE_SENSE
46 VSSCORE_SENSE



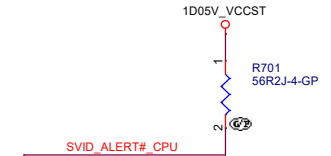
SVID DATA



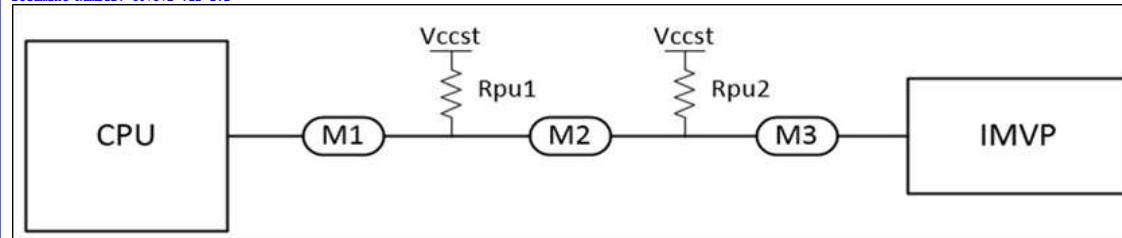
SVID CLOCK



SVID ALERT



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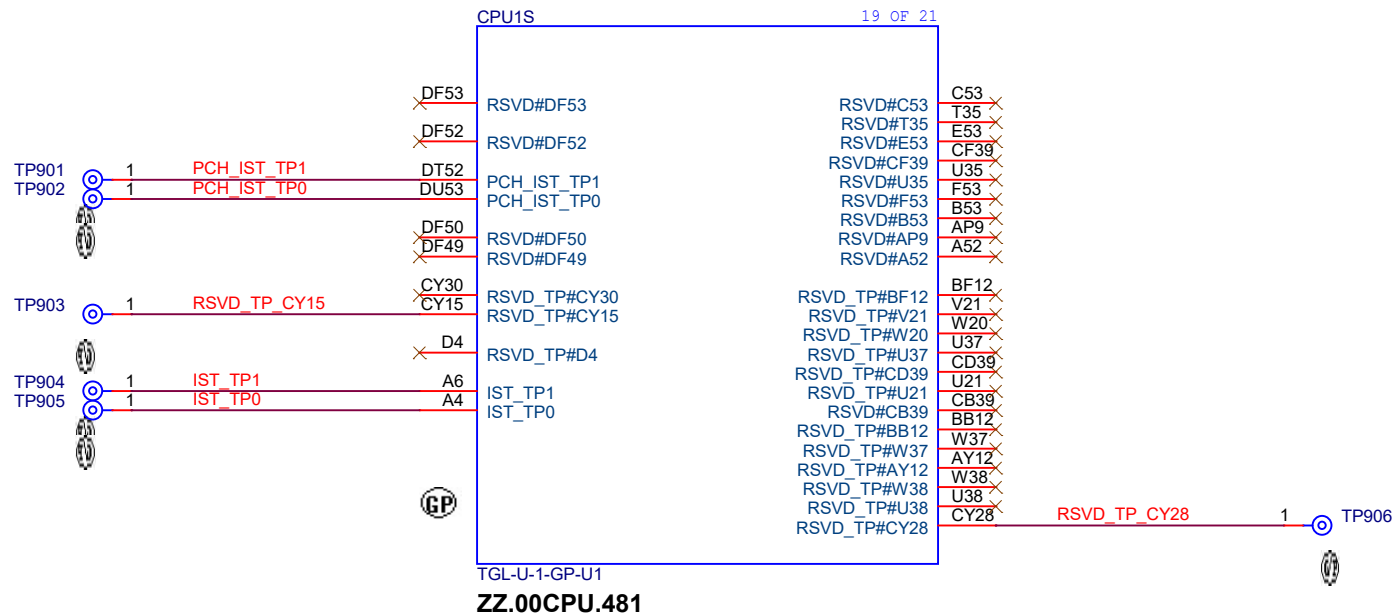


Notes	Details
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSCK platform resistors	Rpu1=empty, Rpu2=45Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=empty
Platform resistors tolerances	5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

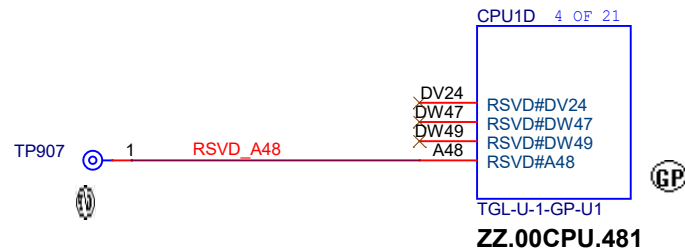
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Title CPU (VCCIN/VID)		
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REFER DOC#614056 FOR ES1 WORKAROUND CIRCUIT FOR PINS CY15 and CY28.



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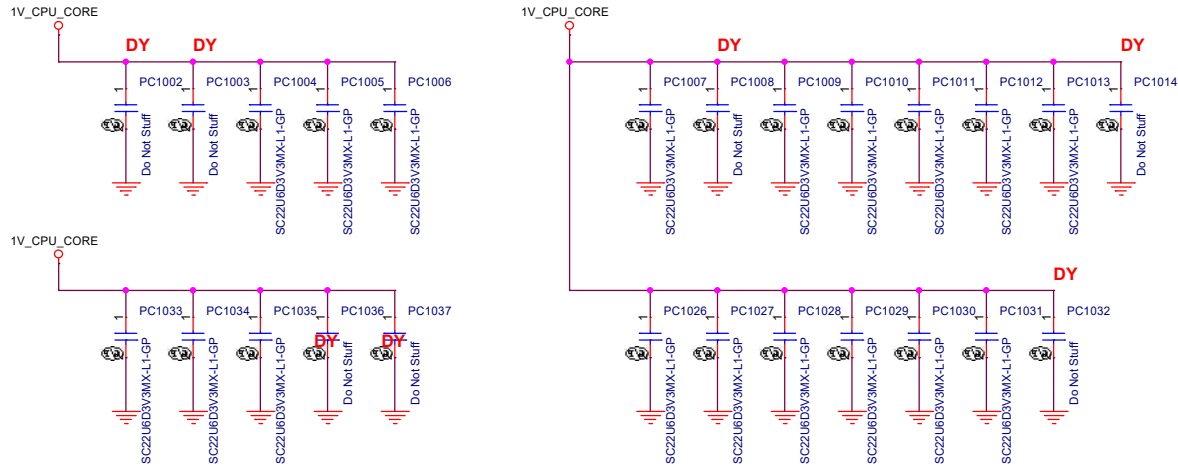
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Title CPU (RSVD)			
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VCORE

TGL_U42

22uF	PCS	Cap
U42	15	330uF*1

U42
IccMax current-10ms max = 65 A



TGL-UP3 8L T3_DS_VCCIN				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN	Secondary Side	0402	10 uF	12
		7343	220 uF	2
	Primary Side	7343	PH	2
		0603	22 uF	8

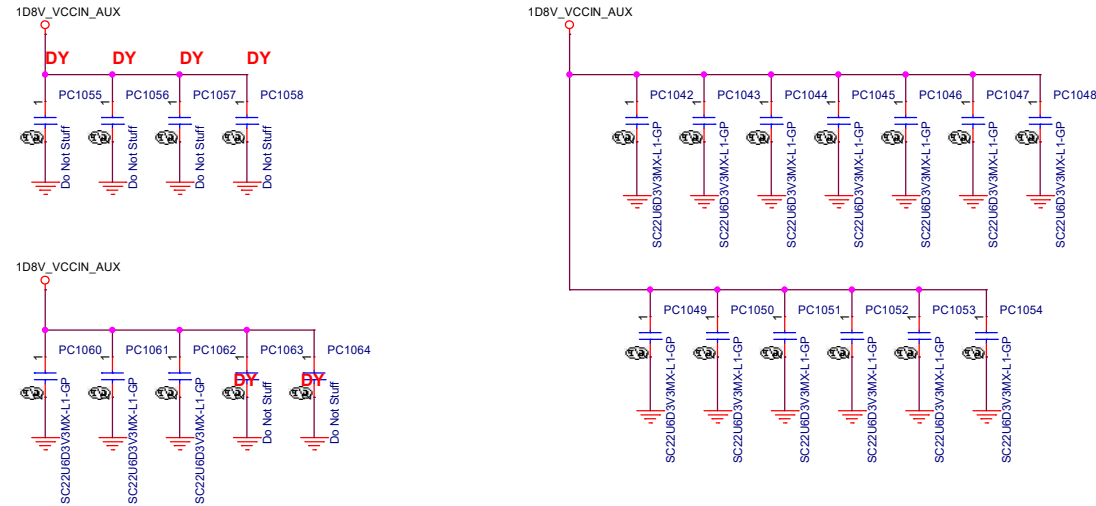
TGL-UP3 8L T3_SS_VCCIN				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN	Primary Side	7343	220 uF	2
		7343	PH	2
		0603	22 uF	10
		0402	10 uF	12

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VCCINAUX

RT6543

22uF	PCS	Cap
U42	13	330uF*1



TGL-UP3 8L T3_DS_VCCIN_AUX				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX	CPU Primary Side	7343	220uF	1
		0805	47uF	3
		0805	Placeholder	3
		0603	22uF	12
		0402	10uF	15
		0402	10uF	10

TGL-UP3 8L T3_SS_VCCIN_AUX				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX	CPU Primary Side	7343	220uF	2
		0805	47uF	3
		0805	Placeholder	3
		0603	22uF	12
		0402	10uF	17

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Title

CPU (CORE Power Cap1)

Size A3

Document Number

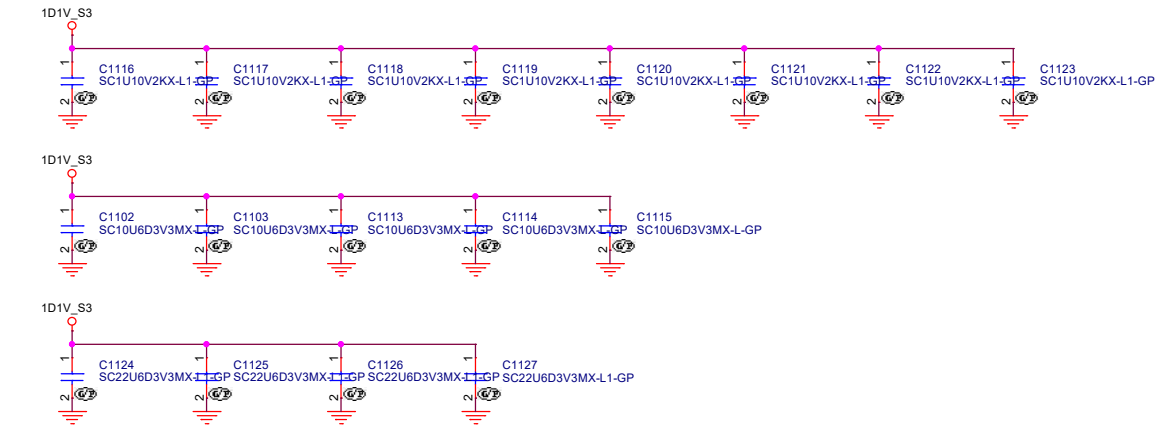
Milgauss_TL

Rev 1

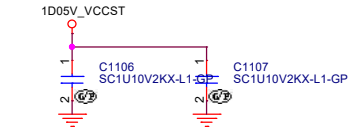
Date: Friday, November 08, 2020

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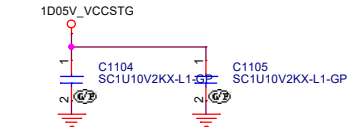
VDDQ



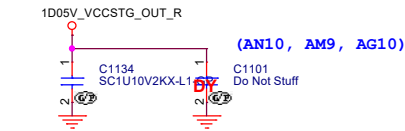
Close to CPU (BT2, BT1, BT4)
VCCST



Close to CPU (BP2, BP1, BP4)
VCCSTG



Close to CPU
(AF12, AD12)



TGL-UP3_8L_T3_DS_VDD2				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCDD2	Secondary Side	0402	10uF	8
	Primary Side	0603	47uF	2
		0402	1uF	8

TGL-UP3_8L_T3_SS_VDD2				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCDD2	Primary Side	0603	47uF	2
		0402	1uF	8
		0402	10uF	13

TGL-UP3_VCCST				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCST	Primary/Secondary Side	0402	1uf	2

TGL-UP3_VCCSTG				
Power Rail	Decap Placement	Form Factor	Value	Number
VCCSTG	Primary/Secondary Side	0402	1uf	2

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Title

CPU (Power Cap2)

Size

Document Number

Rev

A3

Milgauss_TL

1

Date:

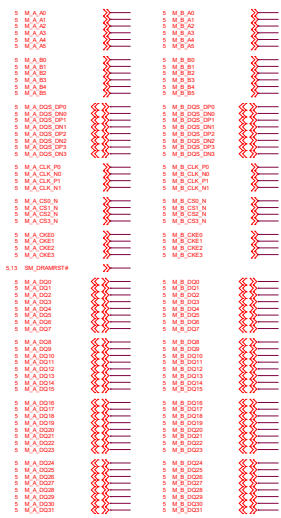
Friday, November 06, 2020

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5.13 SM_DRAWBIST#

5.13 SM_DRAWBIST#

5.13 SM_DRAWBIST#

5.13 SM_DRAWBIST#

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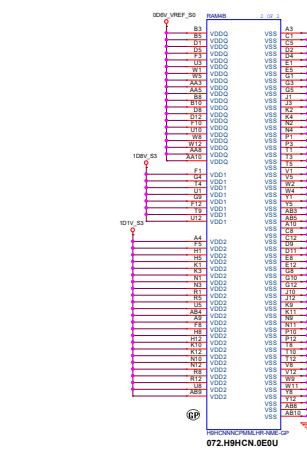
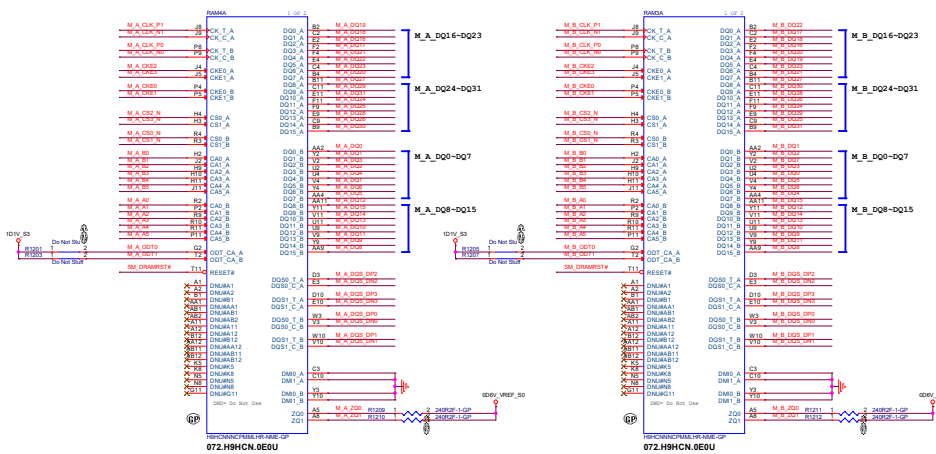
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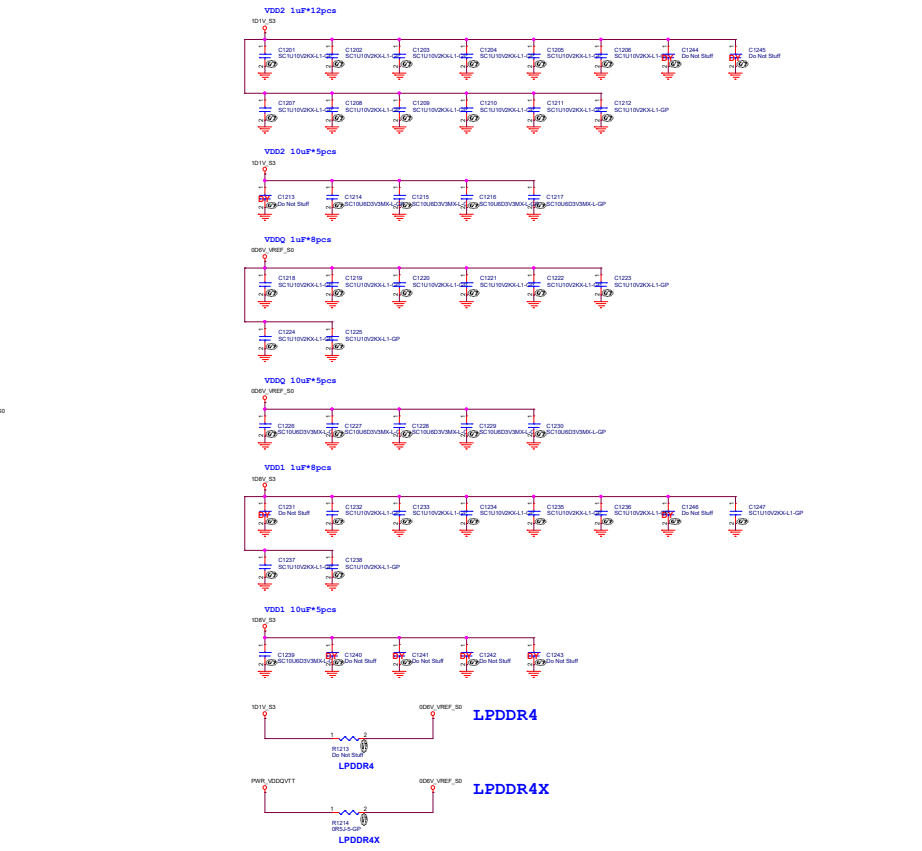
5.13 SM_DRAWBIST#



LPDDR4X Memory Down Power Plane Decoupling

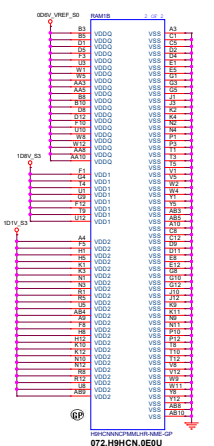
Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4X x32	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1 μ F (0402)
		evenly distribute among all Drams	5x 10 μ F (0603)
	VDDQ	4 per Dram, 2 per short edge	16x 1uF (0402)
		evenly distribute among all Drams	5x 10uF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1 μ F (0402)
		evenly distribute	5x 10 μ F (0603)

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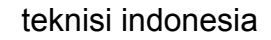
LPDDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4 x32	VDDQ/ VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1 μ F (0402)
		Distribute evenly across domain, close by Drams	6x 10 μ F (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1 μ F (0402)
		distribute evenly across domain, close by Drams	5x 10 μ F (0603)



LPDDR4 Memory Down Power Plane Decoupling

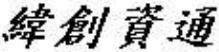
Memory Configuration	Power Domain	Decoupling Location	Qty x μF (size)
LPDDR4 x32	VDDQ/ VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1 μF (0402)
		Distribute evenly across domain, close by Drams	6x 10 μF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1 μF (0402)
		distribute evenly across domain, close by Drams	5x 10 μF (0603)



Blanking

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Title DDR (RSVD)			
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18 GPP_C2/SMBALERT#
18 GPP_C5/SML0ALERT#
18 SPI_SI_CPU
4.72 USB2_TCSS_RXD
4 TBT_LSX3_VCC_CONFIG
18 SPI_WP_CPU
18 SPI_HOLD_CPU
19 HDA_SDOUT_CPU
18 GPP_E6
4.71 USB1_TCSS_RXD
4 TBT_LSX1_VCC_CONFIG
3 DBG_PMODE
21 CNV_BRI_DT_R
21 CNV_RGI_DT_R
17 SPI_VCC_SEL

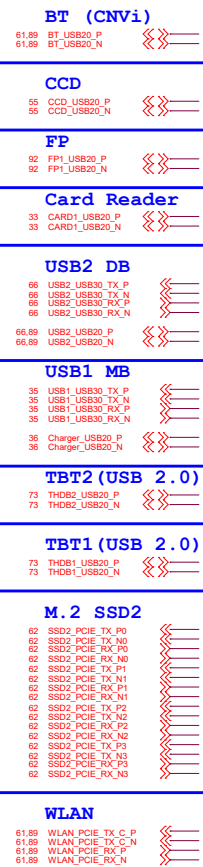
Description	Top Swap Override	No Reboot	TL8 Confidentiality	Boot Strap 0	Reserved	DDP3 I2C / TBT_LSX2 / BSSB LS2 pins VCC configuration	DDP4 I2C / TBT_LSX3 / BSSB LS3 pins VCC configuration	CPUNSSC Clock Frequency
GPIO	GPP_B14	GPP_B18	GPP_C2	GPP_C5	SPI0_MOSI	GPP_D10	GPP_D12	GPP_B23
Schematics								
High	Enable	Enable	Enable			3.3V	3.3V	19.2MHz CLOCK FROM DIVIDER (DERIVED FROM 38.4MHz CRYSTAL)
Low	Disable	Disable	Disable			1.8V	1.8V	38.4 MHz clock (Direct from crystal)
	internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%		internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%

Description	Reserved	Reserved	Flash Descriptor Security Override	JTAG ODT Disable	DDP1 I2C / TBT_LSX0 / BSSB LS0 pins VCC configuration	DDP2 I2C / TBT_LSX1 / BSSB LS1 pins VCC configuration	Reserved	Reserved
GPIO	SPI0_IO2	SPI0_IO3	GPP_R2	GPP_E6	GPP_E19	GPP_E21	DBG_PMODE	GPD7
Schematics								
High			Disable	Enable	3.3V	3.3V		
Low			Enable	Disable	1.8V	1.8V		
			internal pull-down 20 kohm \pm 30%		internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%	internal pull-up 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%

Description	XTAL Frequency Selection	M.2 CNVi Mode Select	Reserved	Reserved	Boot Strap1	Boot Strap2	Boot Strap3	SPI Operation Voltage Select
GPIO	GPP_F0	GPP_F2	GPP_F7	GPP_F10	GPP_H0	GPP_H1	GPP_H2	SPIVCCIOSEL
Schematics					Bit1	Bit2	Bit3	
High	24 MHz	Disable						SPI = 1.8V
Low	38.4 MHz	Enable						SPI = 3.3V
	internal pull-down 20 kohm \pm 30%		internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%	internal pull-down 20 kohm \pm 30%			

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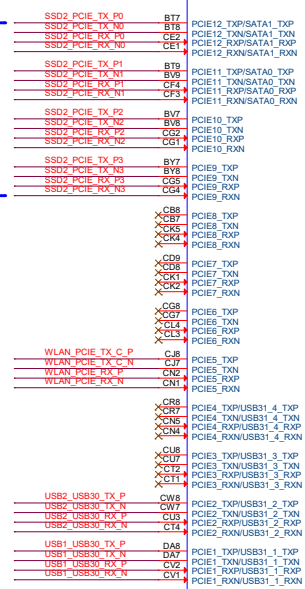
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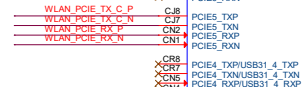
SSID= PCH

Document Number: 576551 Ver 1.2
Document Number: 607872 Ver 1.1

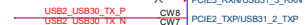
M.2 SSD2 (PCIe/SATA)



WLAN



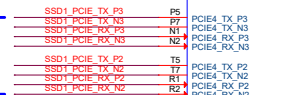
USB2 (USB 3.0) DB



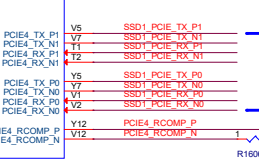
USB1 (USB 3.0) MB



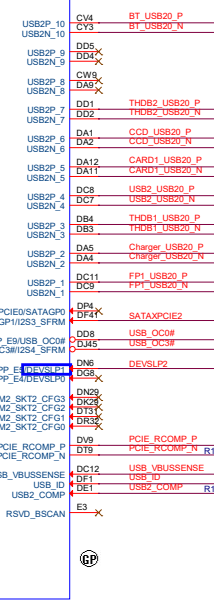
M.2 SSD1 (PCIe)



M.2 SSD1 (PCIe)



BT (CNVi)



TBT2 (USB 2.0)

CCD

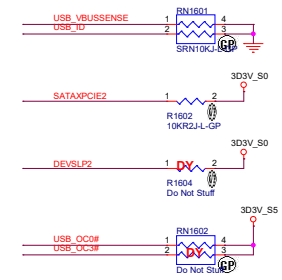
Card Reader

USB2 (USB 2.0) DB

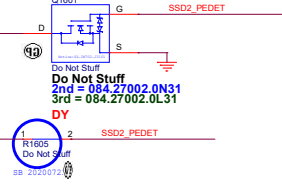
TBT1 (USB 2.0)

USB1 (USB 2.0) MB

FP



M.2 auto detection



Features	Premium UP3	Premium UP4
USB 2.0 Ports	10	10
PCIe Gen 3 Lanes	12	10
PCIe Root Ports	6	5
USB 3.2 Gen 2x1 Ports	4	4
SATA Ports (all 6 Gb/s capable)	2	0
AUDIO DSP Core Count	4	4

SKU	0	1	2	3	4	5	6	7	8	9	10	11
Premium UP3	USB 3.2 Gen 2x1/PCIe 3.0	USB 3.2 Gen 2x1/PCIe 3.0	USB 3.2 Gen 2x1/PCIe 3.0	USB 3.2 Gen 2x1/PCIe 3.0	PCIe 3.0	PCIe 3.0	PCIe 3.0/GbE	PCIe 3.0/GbE	PCIe 3.0/GbE	PCIe 3.0	PCIe 3.0/SATA	PCIe 3.0/SATA
Premium UP4	USB 3.2 Gen 2x1/PCIe 3.0	USB 3.2 Gen 2x1/PCIe 3.0	USB 3.2 Gen 2x1/PCIe 3.0	USB 3.2 Gen 2x1/PCIe 3.0	-	-	PCIe 3.0/GbE	PCIe 3.0/GbE	PCIe 3.0/GbE	PCIe 3.0	PCIe 3.0	PCIe 3.0

CHIPSET SKU	Max USB 2.0 Nbr of Ports	USB 2.0 P1	USB 2.0 P2	USB 2.0 P3	USB 2.0 P4	USB 2.0 P5	USB 2.0 P6	USB 2.0 P7	USB 2.0 P8	USB 2.0 P9	USB 2.0 P10 (for CNVi/BT)	USB1	USB2
PREMIUM-UP4	6												
PREMIUM-UP3	10												
MAINSTREAM BASE-UP3	8												

Port Disabled

Port Enabled

Port Enabled for Intel® Wireless-AC only

Integrated Bluetooth* and USB 2.0 Design Considerations

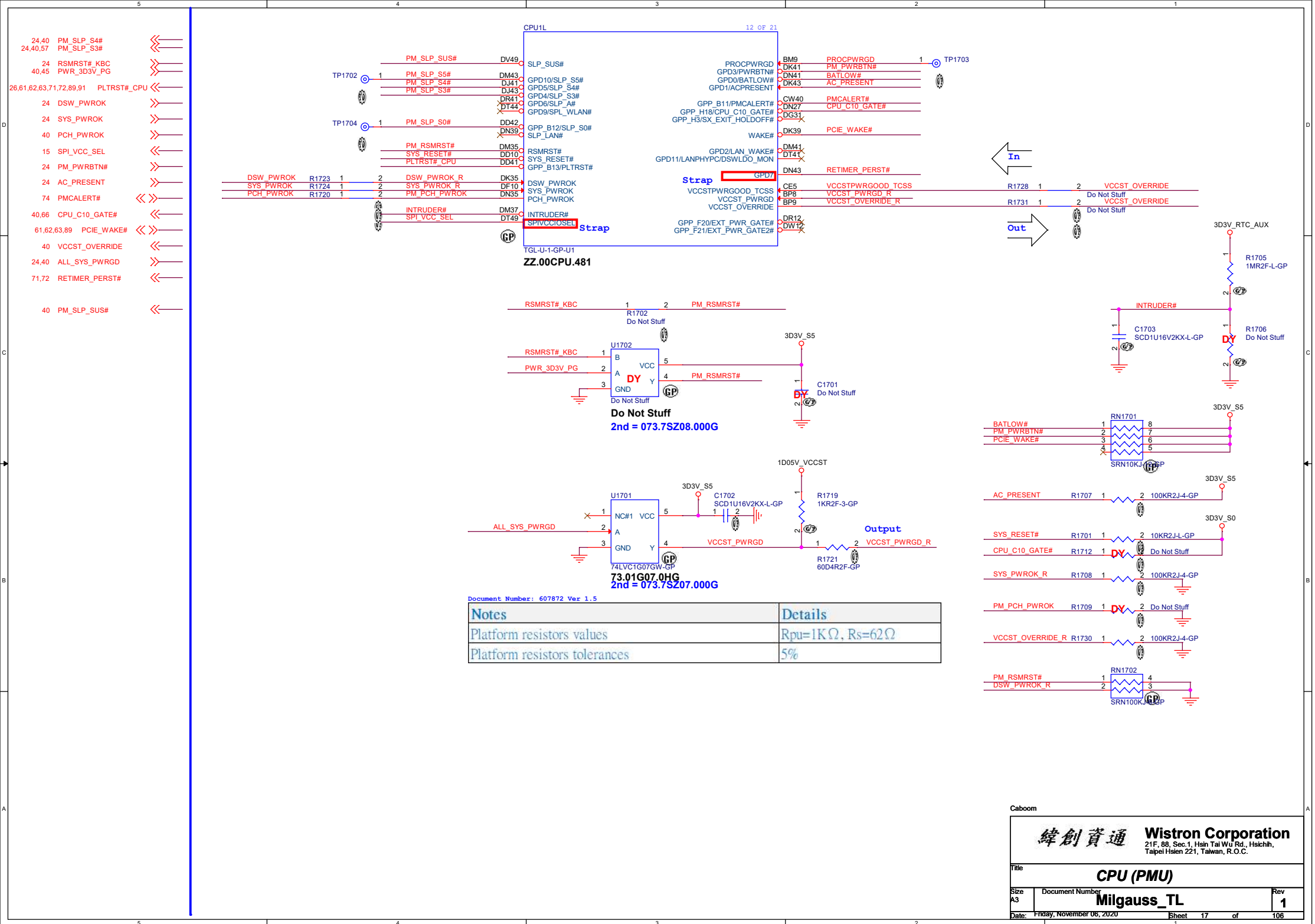
Tiger Lake UP3

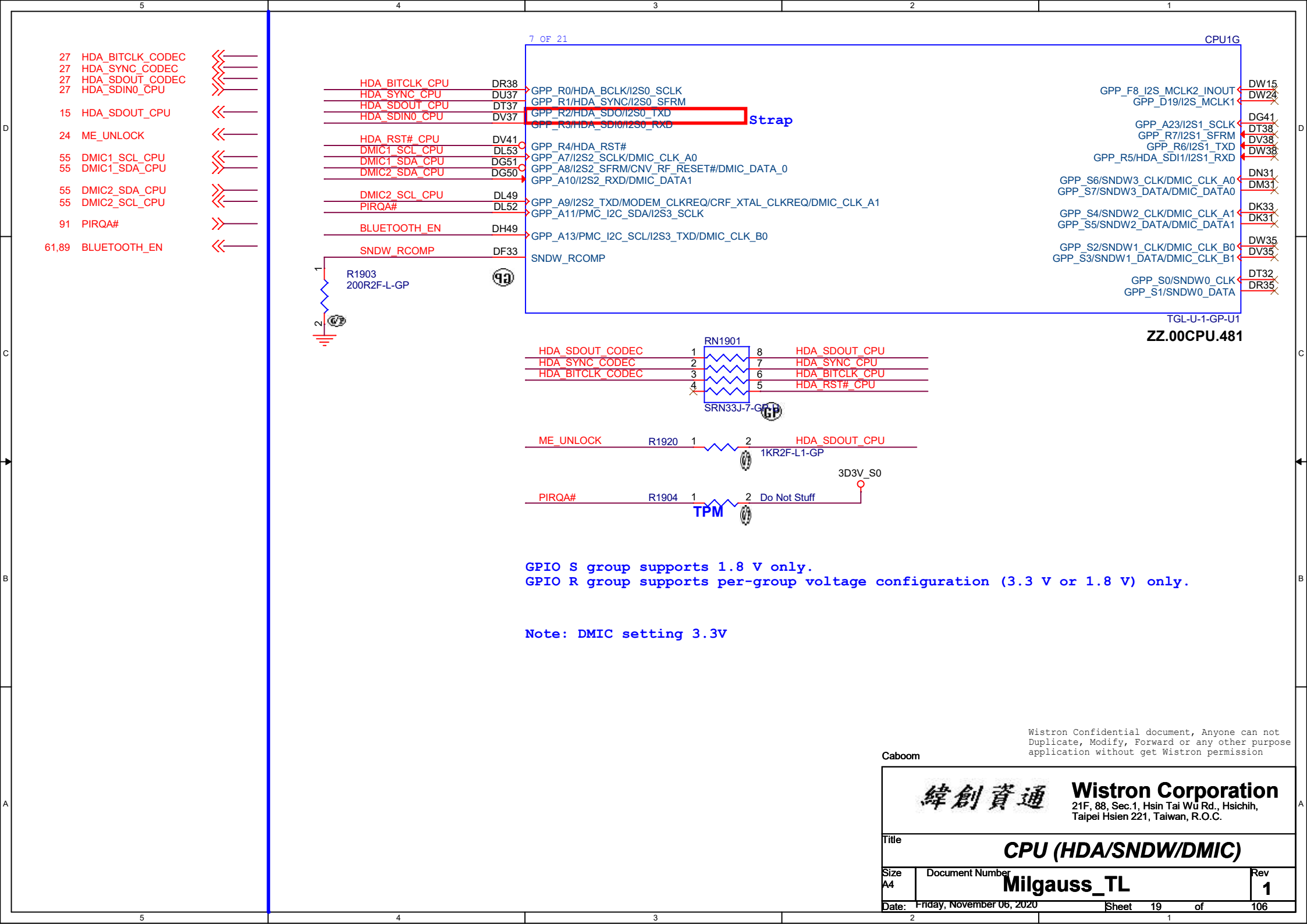
For integrated Bluetooth* functionality with the Intel® Wireless-AC (CNVi) solution, Tiger Lake PCH-LP USB 2.0 port # 10 must be used.

If integrated Bluetooth* functionality is not desired, Tiger Lake UP3 USB 2.0 port 10 may be used for USB functionality.

PCH-LP	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3
Flex I/O Lanes	0 1 2 3	4 5 6 7	8 9 10 11
PCIe* Lanes	1 2 3 4	5 6 7 8	9 10 11 12
Logical Link Lanes	1x4 LR 0 1 2 3 2x2 LR 0 1 0 1 2x2 LR 1 0 1 0 1x2+2x1 0 1 0 0 2x1+1x2 0 0 1 0 4x1 0 0 0 0	0 1 2 3 4 5 6 7 8 9 10 11 12 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 0 1 0 1 0	0 1 2 3 4 5 6 7 8 9 10 11 12 0 1 2 3 4 5 6 7 8 9 10 11 12 0 1 2 3 4 5 6 7 8 9 10 11 12 0 1 2 3 4 5 6 7 8 9 10 11 12 0 1 2 3 4 5 6 7 8 9 10 11 12 0 1 2 3 4 5 6 7 8 9 10 11 12
Assigned Root Ports	1x4 LR RP1 2x2 RP1 RP3 2x2 LR RP3 RP1 1x2+2x1 RP1 RP3 RP4 2x1+1x2 RP4 RP3 RP1 4x1 RP1 RP2 RP3 RP4	RP5 RP7 RP5 RP7 RP5 RP7 RP5 RP7 RP5 RP7 RP5 RP7	RP9 RP11 RP9 RP11 RP9 RP11 RP9 RP11 RP9 RP11 RP9 RP11

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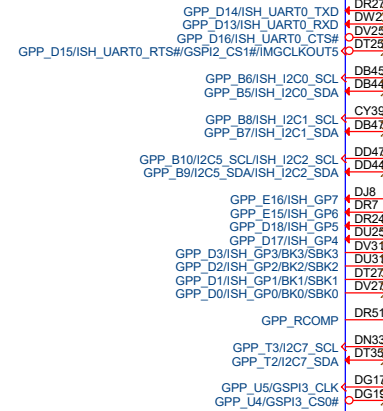
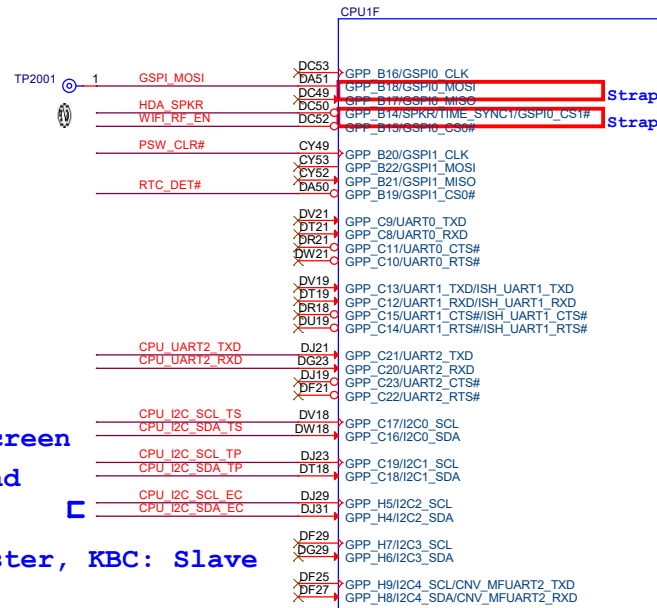




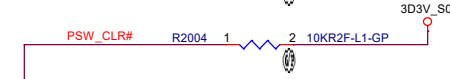
- 27 HDA_SPKR <<
61,89 WIFI_RF_EN <<
25 RTC_DET# >>
68 CPU_UART2_TXD <<
68 CPU_UART2_RXD <<
55 CPU_I2C_SCL_TS <<
55 CPU_I2C_SDA_TS <<
65 CPU_I2C_SCL_TP <<
65 CPU_I2C_SDA_TP <<
24 CPU_I2C_SCL_EC <<
24 CPU_I2C_SDA_EC <<
24 EC_SCI# <<

Touch Screen
Touch Pad

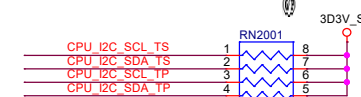
CPU: Master, KBC: Slave



R2002 BIOS Internal Pull Up.



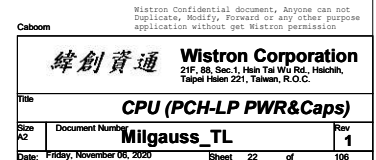
G2001
Do Not Stuff
Password Clear



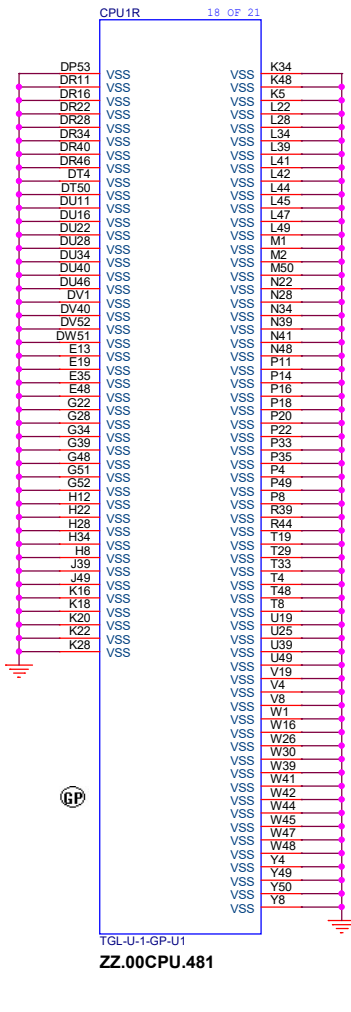
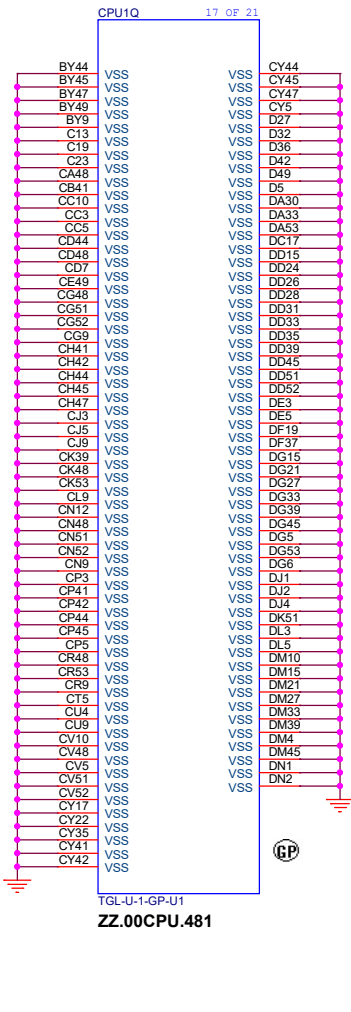
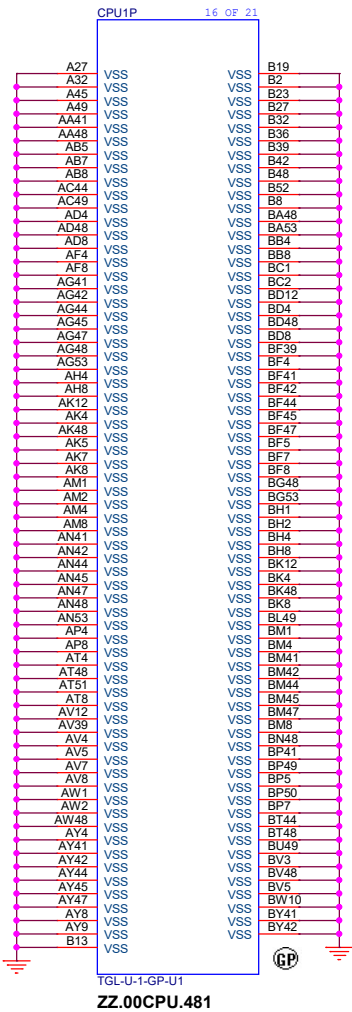
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Title CPU (UART/I2C/ISH)			
Size A3	Document Number	Rev 1	
Date: Friday, November 08, 2020		Sheet 20	of 106



VCCPRIM_1P05	Loopback 1P05 Power to supply to CNVPLL and CNVLDO	This rail does not connect to external voltage regulator. It is a loop-back power rail supported by PCH itself.
VCC1P05	Loopback 1P05 Power to Supply to CPU Load (PLL, ST, STG, FETs)	This rail does not connect to external voltage regulator. It is a loop-back power rail supported by PCH itself to CPU load.
VCCLDOSTD_0P85	Decap connection only	
VCCDSW_1P05	Decap connection only	
VCCDPHY_1P24	Decap connection only	



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Title CPU (VSS)		
Size A3	Document Number Milgauss_TL	Rev 1
Date: Friday, November 06, 2020	Sheet 23 of	106

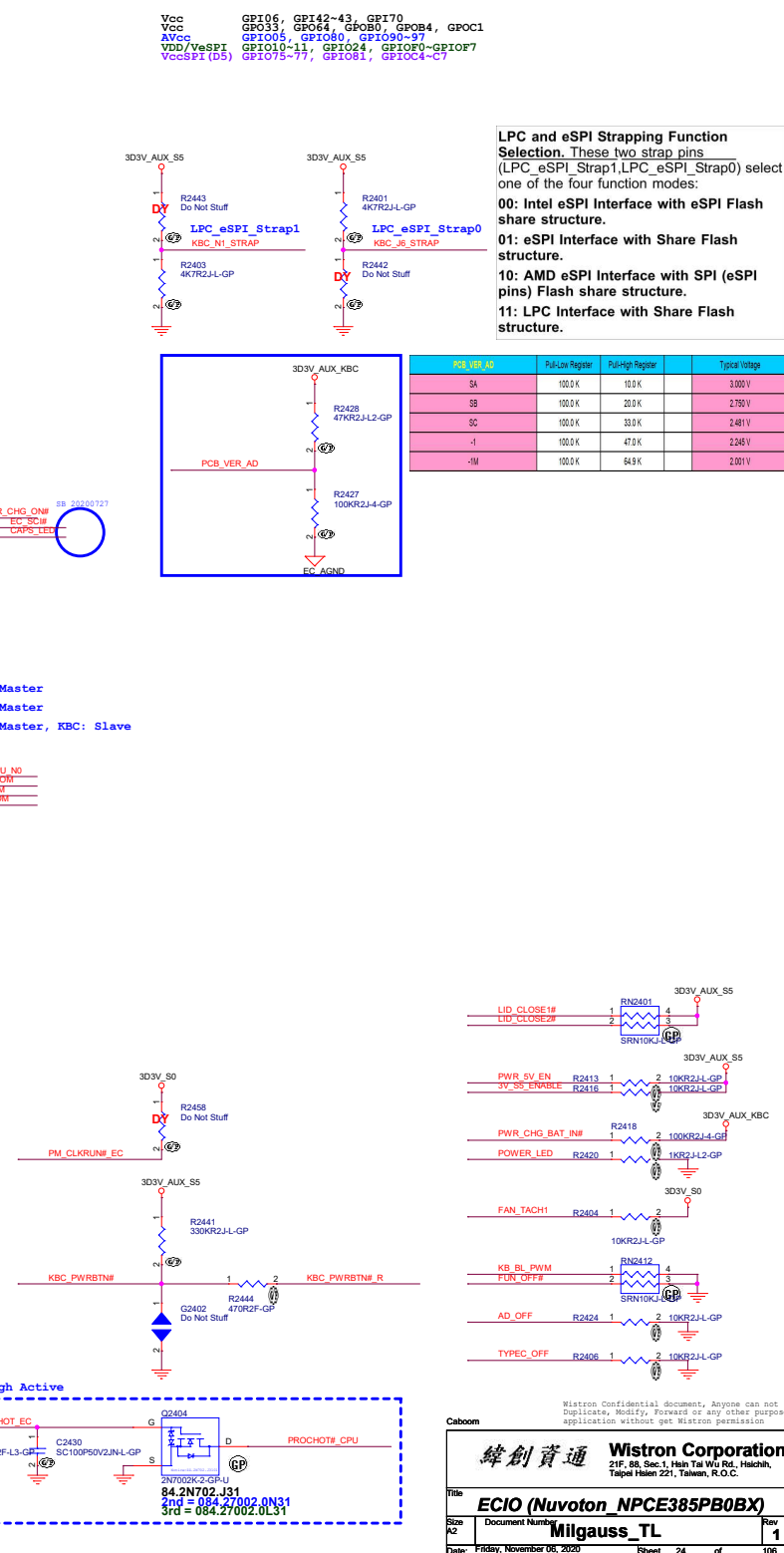
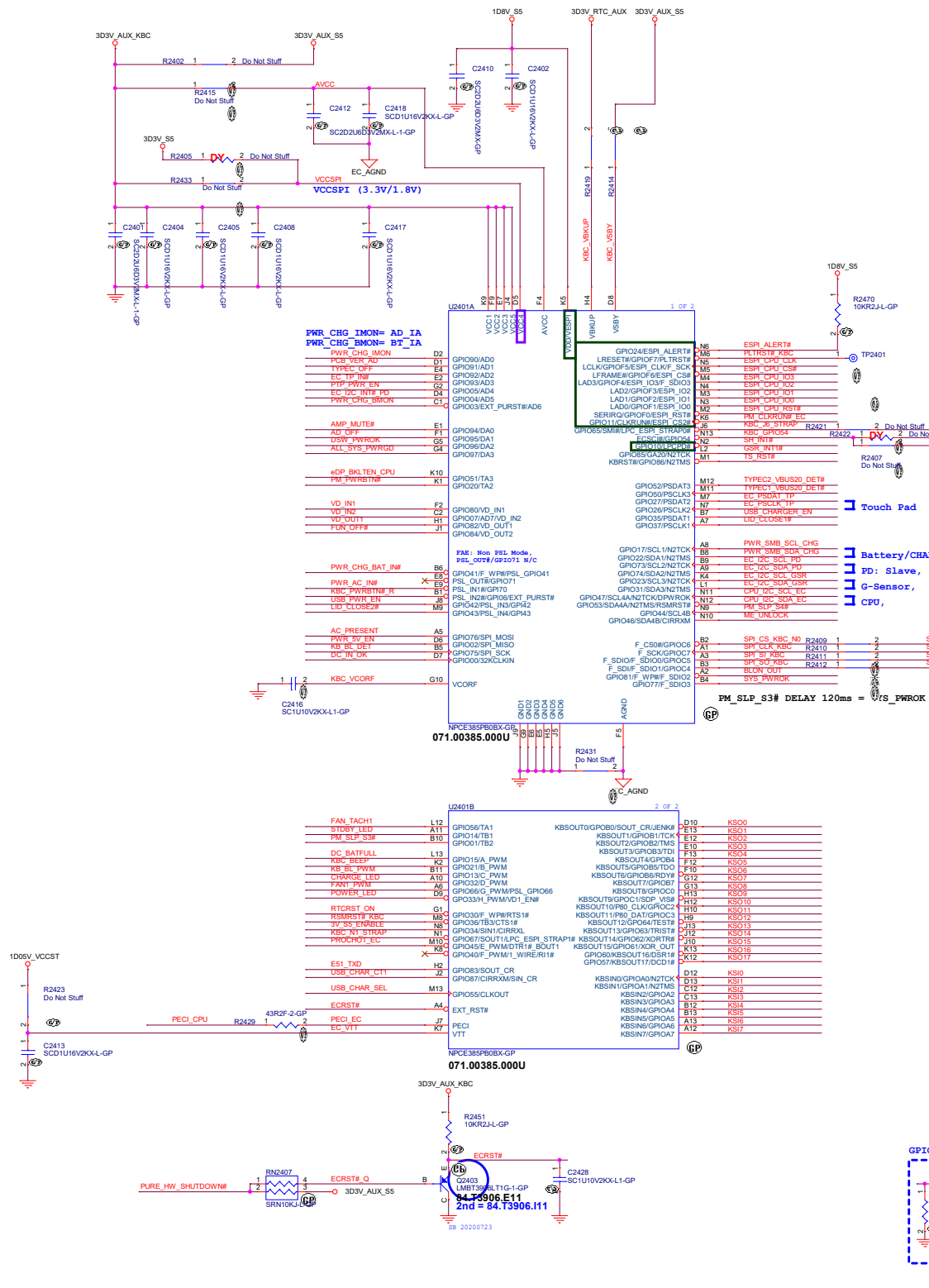
SSID = KBC

44 PWR_CHG_IMON
44 TYPEC_OFF
65 EC_TP_IN#
65 PTP_PWR_EN
74 EC_IC_SDA_PD
44 PWR_CHG_BMON
27 AMP_MUTE#
44.74 AD_OFF
17 DSUV_PWRKOK
17 ALL_SYS_PWRGD
4 eDP_BKLTEN_CPU
17 PM_PWRBTN#
26 VD_IN1
26 VD_IN2
26 VD_OUT1
65.89 FUN_OFF#
43.44 PWR_CHG_BAT_IN#
44 PWR_AC_IN#
64.66.89 KBC_PWRBTN#
66 USB_PWR_EN
66.89 LID_CLOSE#
17 AC_PRESENT
45 PWR_SV_EN
65 KB_BL_DET
43.74 DC_INOK
68. ESPI_ALERT#
26.61,62,63,17,2,26.51 PLTRST# CPU
18.68 ESPI_CPU_CLK
18.68 ESPI_CPU_CS#
18.68 ESPI_CPU_IO3
18.68 ESPI_CPU_IO2
18.68 ESPI_CPU_IO1
18.68 ESPI_CPU_IO0
18.68 ESPI_CPU_RST#
44 PWR_CHG_ON#
20 EC_SC#
65 CAPS_LED
3 SH_INT#
66.70 GSR_INT#
65 TS_RST#
42 TYPEC2_VBUS2_DET#
42 TYPEC1_VBUS2_DET#
65 EC_PSDAT_TP
65 EC_PSLCK_TP
36 USB_CHARGER_EN
66 LID_CLOSE#
43.44 PWR_SMB_SCL_CHG
43.44 PWR_SMB_SDA_CHG
74 EC_IC_SCL_PD
74 EC_IC_SDA_PD
66.70 EC_IC_SCL_GSR
66.70 EC_IC_SDA_GSR
20 CPU_IC_SCL_EC
20 CPU_IC_SDA_EC
17.40 PM_SLP_S#
19 ME_UNLOCK
18.25 SPI_CS_CPU_N0
18.25.91 SPI_CLK_ROM
18.25.91 SPI_S1_ROM
18.25.91 SPI_S0_ROM
17 SYS_PWRKOK
55 BLON_OUT
26 FAN_TACH1
66.89 STDBY_LED
17.40.57 PM_SLP_S#
66.89 DC_BATFULL
27 KBC_BEEP
65 KB_BL_PWM
66.89 CHARGE_LED
26.89 FAN1_PWM
66.89 POWER_LED
18 RTDST_CN
17 RSMRST#_KBC
40 3V_SS_ENABLE
PROCHOT#_CPU
61.68 ES1_TXD
36 USB_CHAR_CT1
36 USB_CHAR_SEL
26.40 PURE_HW_SHUTDOWN#
3 PECL_CPU
65.89 KS00
65.89 KS01
65.89 KS02
65.89 KS03
65.89 KS04
65.89 KS05
65.89 KS06
65.89 KS07
65.89 KS08
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26 FAN_TACH1
66.89 STDBY_LED
17.40.57 PM_SLP_S#
66.89 DC_BATFULL
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66.89 CHARGE_LED
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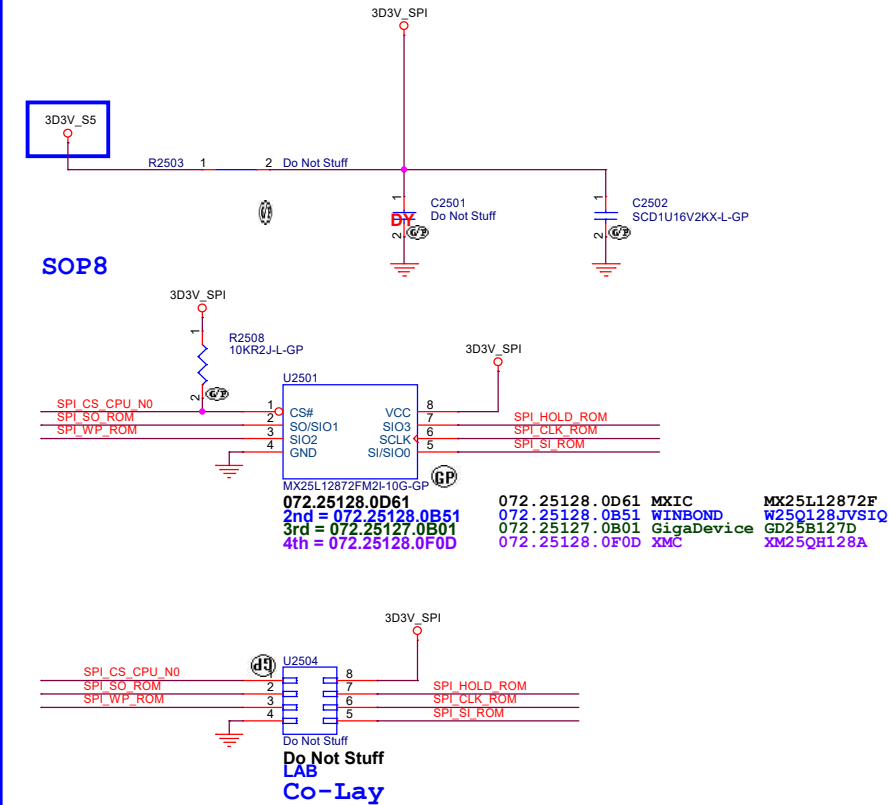
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66.89 POWER_LED
18 RTDST_CN
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36 USB_CHAR_CT1
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65.89 KS00
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26 FAN_TACH1
66.89 STDBY_LED
17.40.57 PM_SLP_S#
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65 KB_BL_PWM
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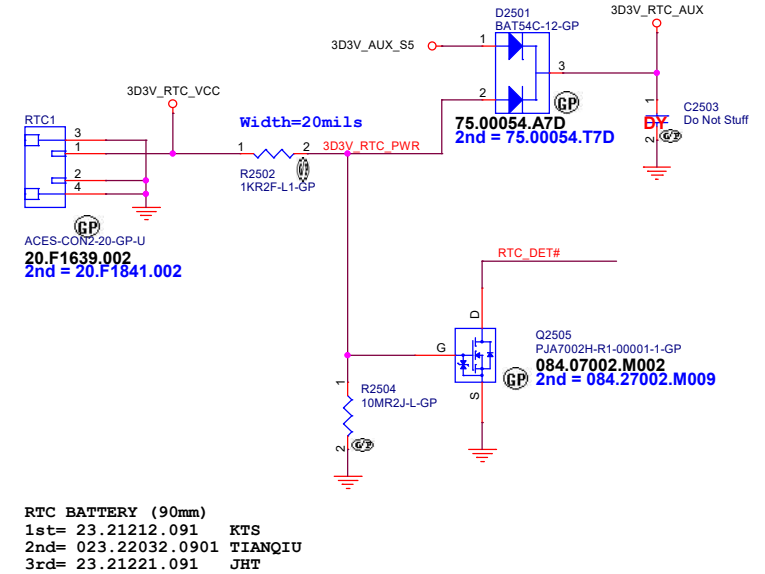


Main Func = SPI Flash

SPI Flash ROM (16M Byte)



Main Func = RTC



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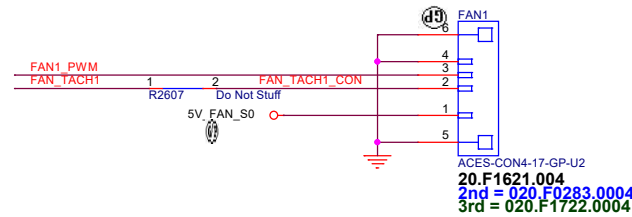
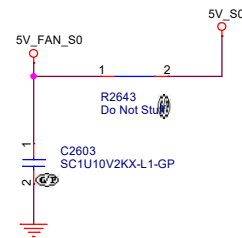
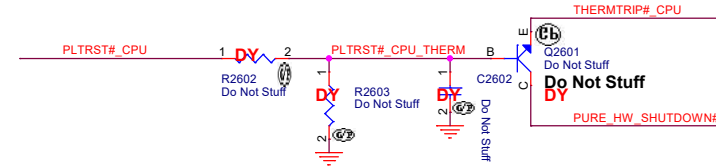
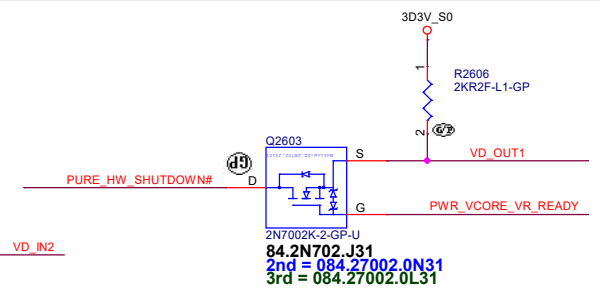
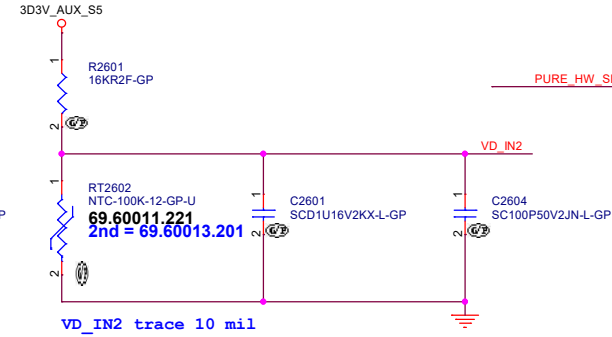
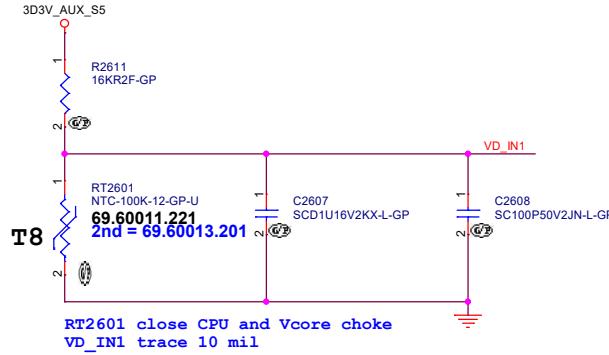
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Title			
Flash/RTC			
Size	Document Number	Rev	
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SSID = Thermal

24 VD_IN1
24 VD_IN2
24,40 PURE_HW_SHUTDOWN#
24 VD_OUT1
40,46 PWR_VCORE_VR_READY

24,89 FAN1_PWM
24 FAN_TACH1
89 FAN_TACH1_CON

33,71,72,89,91 PLTRST# CPU
3 THERMTRIP#_CPU



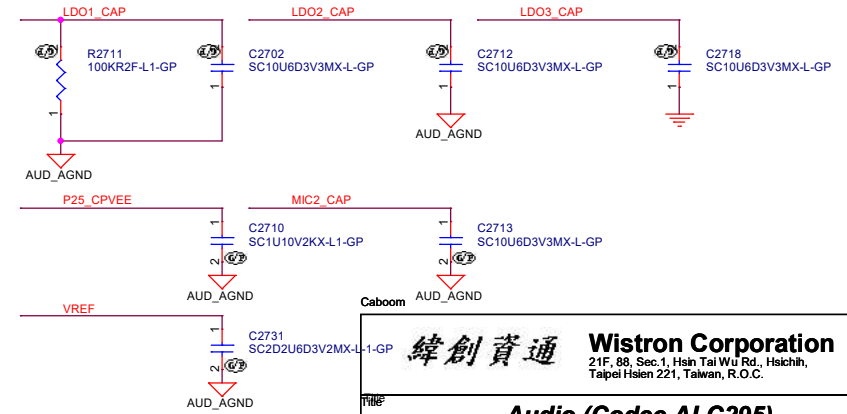
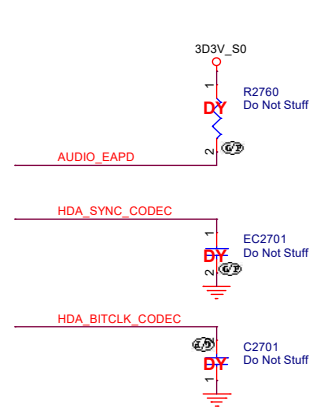
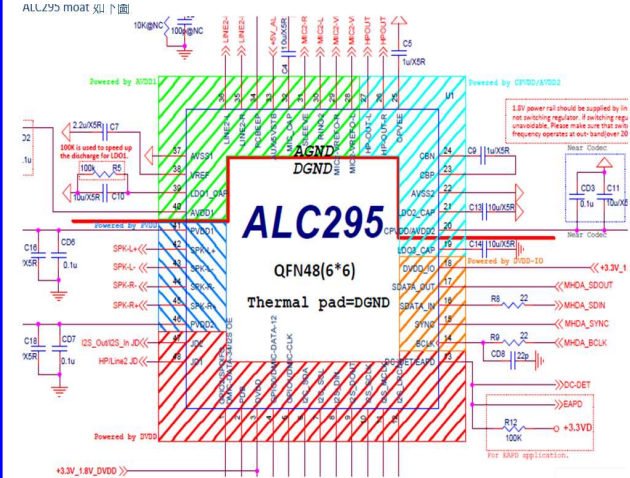
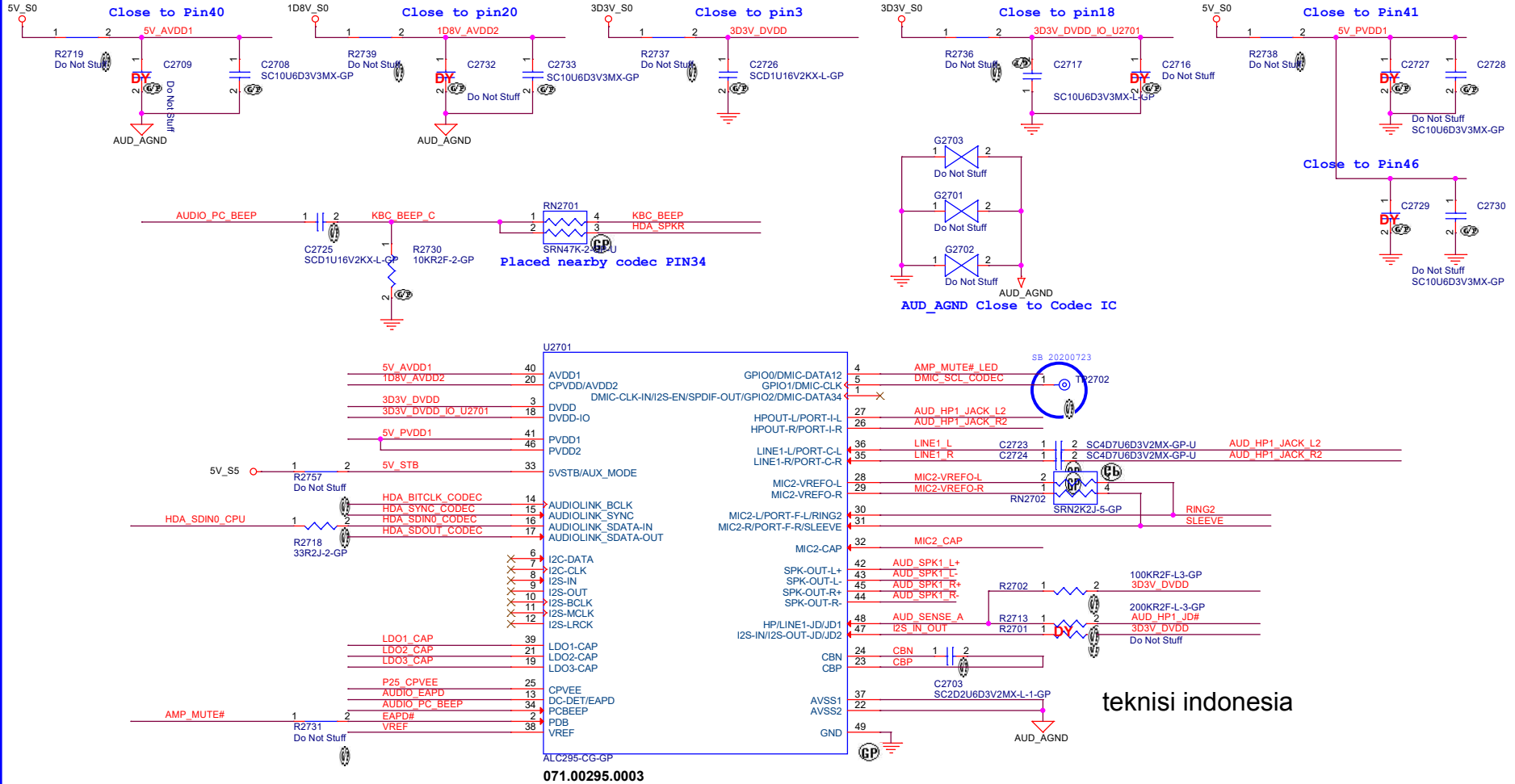
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Title			
INT IO (Thermal/Fan)			
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SSID = AUDIO

- 19 HDA_SYNC_CODEC
- 19 HDA_BITCLK_CODEC
- 19 HDA_SDOUT_CODEC
- 19 HDA_SIN0_CPU
- 24 KBC_BEEP
- 20 HDA_SPKR
- 24 AMP_MUTE#
- 66,89 AUD_HP1_JACK_L2
- 66,89 AUD_HP1_JACK_R2
- 66,89 RING2
- 66,89 SLEEVE
- 66 AUD_HP1_JD#
- 29 AUD_SPK1_L+
- 29 AUD_SPK1_L-
- 29 AUD_SPK1_R+
- 29 AUD_SPK1_R-
- 65 AMP_MUTE#_LED



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Audio (Codec ALC295)

Milgauss_TL

Rev 1

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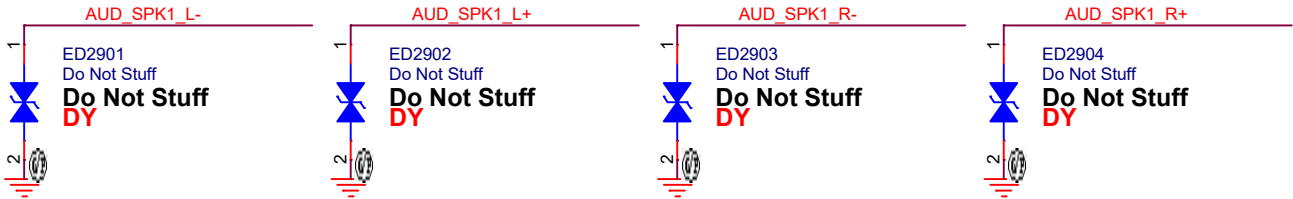
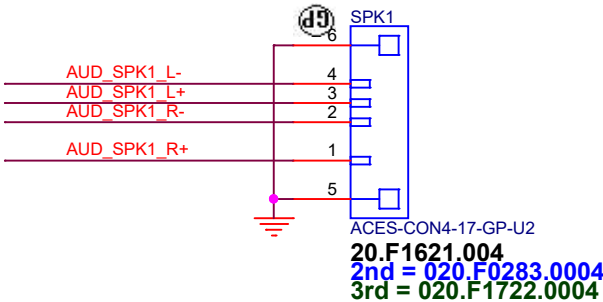
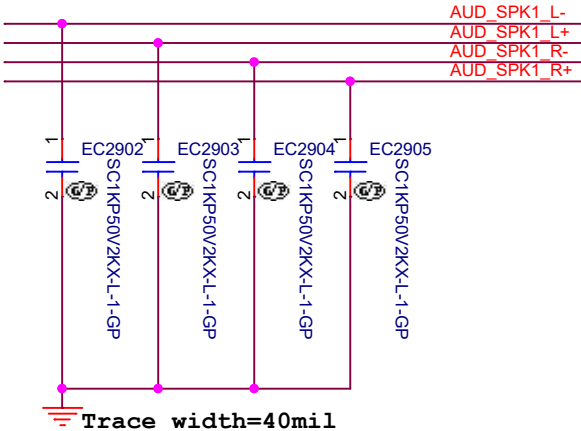
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Title <div>Audio (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Milgauss_TL</div>	Rev <div>1</div>
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27 AUD_SPK1_L-
27 AUD_SPK1_L+
27 AUD_SPK1_R-
27 AUD_SPK1_R+



SSID = AUDIO

Speaker



ALC295:

		DVDD (1.8V/3.3V) (mA)	DVDD-IO (1.5V/3.3V) (mA)	AVDD1 (5V) (mA)	AVDD2+CPVDD (1.8V) (mA)	PVDD1/2 (5V) (mA)
1	DVDD=1.8V, DVDD-IO=1.5V	10	5	50	200	1500
2	DVDD=3.3V, DVDD-IO=3.3V	10	5	50	200	1500

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Title

Audio (SPK)

Size

Document Number

Rev

A4

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1

Date:

Friday, November 06, 2020

Sheet

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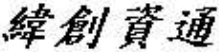
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Title <div>Audio (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Milgauss_TL</div>	Rev <div>1</div>
Date: Friday, November 06, 2020		Sheet 30 of 106

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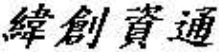
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Title LAN (RSVD)			
Size A4	Document Number Milgauss_TL		Rev 1
Date: Friday, November 06, 2020		Sheet 31 of	106

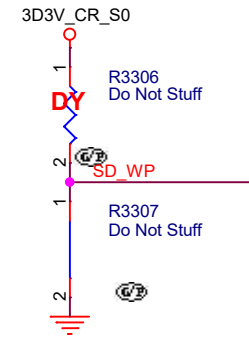
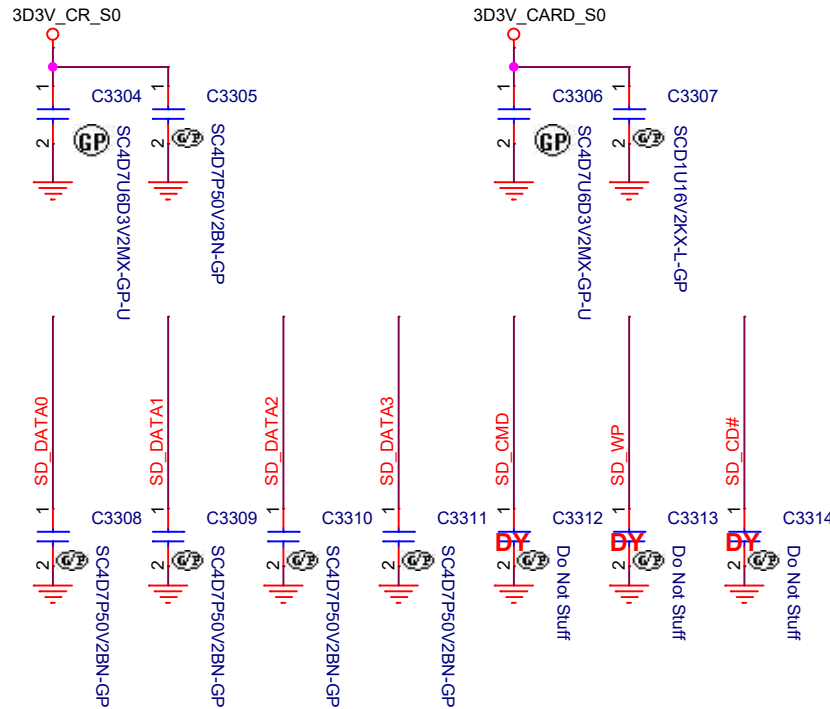
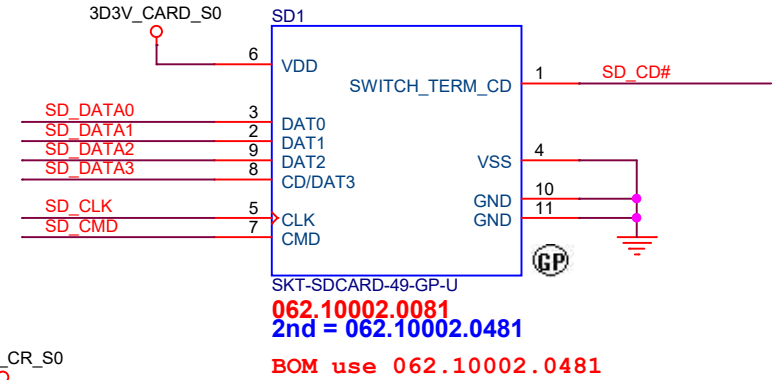
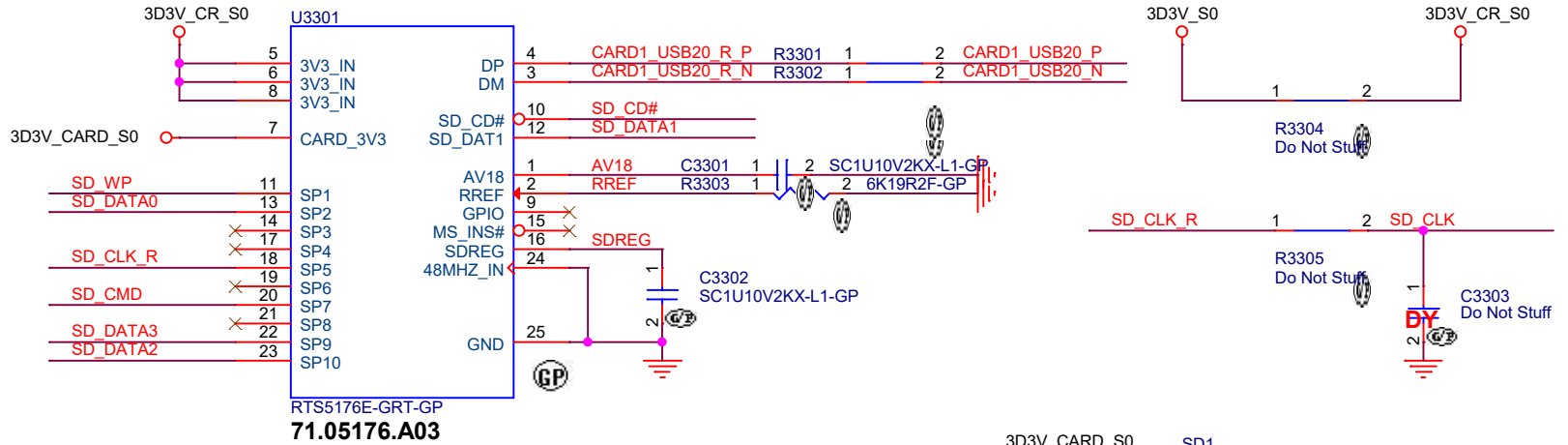
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Title			
LAN (RSVD)			
Size	Document Number		Rev
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16 CARD1_USB20_P
16 CARD1_USB20_N
89 CARD1_USB20_R_P
89 CARD1_USB20_R_N



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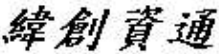
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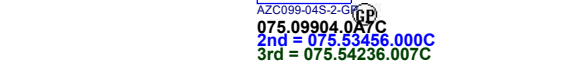
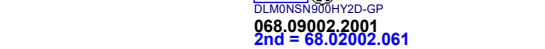
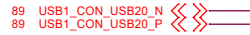
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Title USB (RSVD)			
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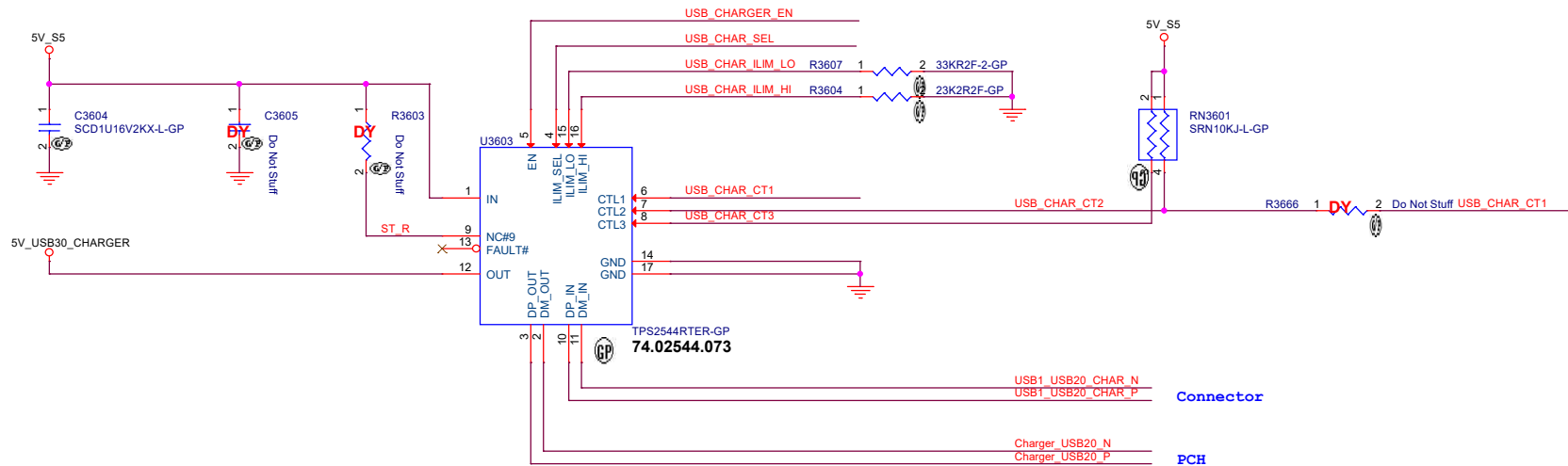


9	<i>StdA_SSTX+</i>
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24 USB_CHARGER_EN >>>
24 USB_CHAR_SEL >>>
24 USB_CHAR_CT1 >>>
PCH
16 Charger_USB20_N <<<
16 Charger_USB20_P <<<
Connector
35 USB1_USB20_CHAR_N <<<
35 USB1_USB20_CHAR_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	Data Lines
0	0	1	0	DCP_Auto	ILIM_HI	Disconnected
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines
1	1	0	1	SDP1	ILIM_HI	Connected
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data Lines Connected

S5 (at low battery and non support charger)

S3 and S5 state

S0 and S3 (at low battery and non support charger)

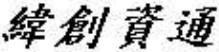
S0 state

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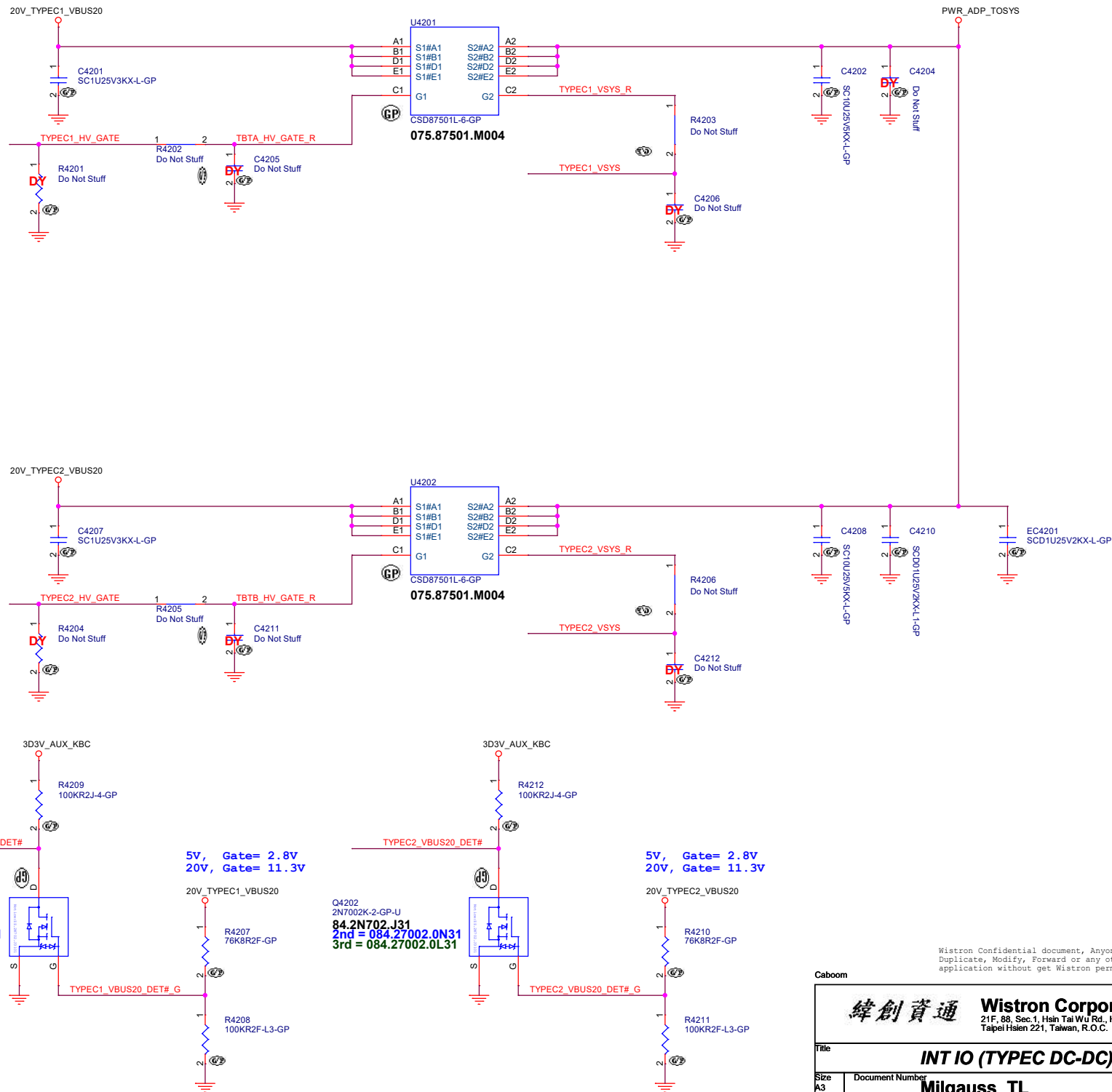
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Title <div>Sequence (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Milgauss_TL</div>	Rev <div>1</div>
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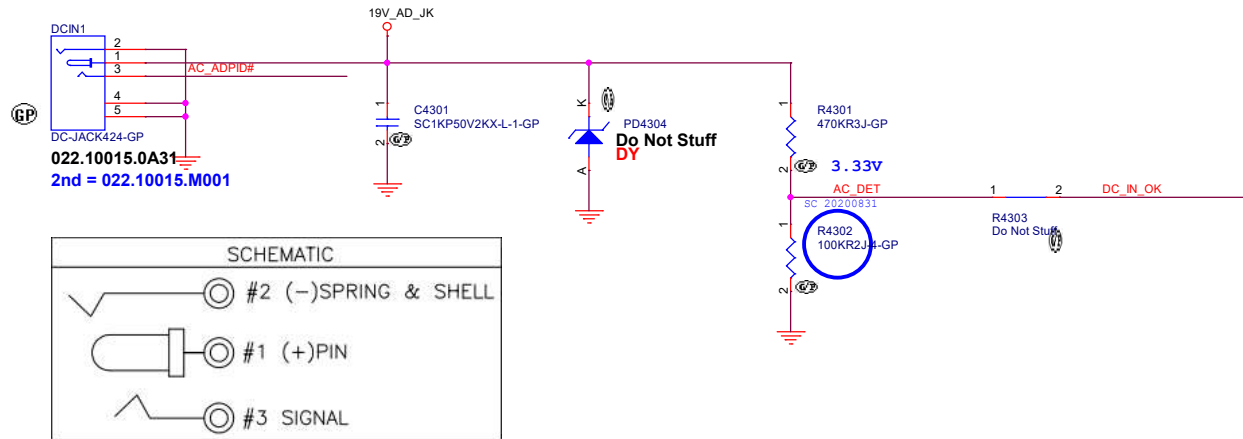
74 TYPEC1_HV_GATE
74 TYPEC2_HV_GATE
24 TYPEC1_VBUS20_DET#
24 TYPEC2_VBUS20_DET#
74 TYPEC1_VSYS
74 TYPEC2_VSYS



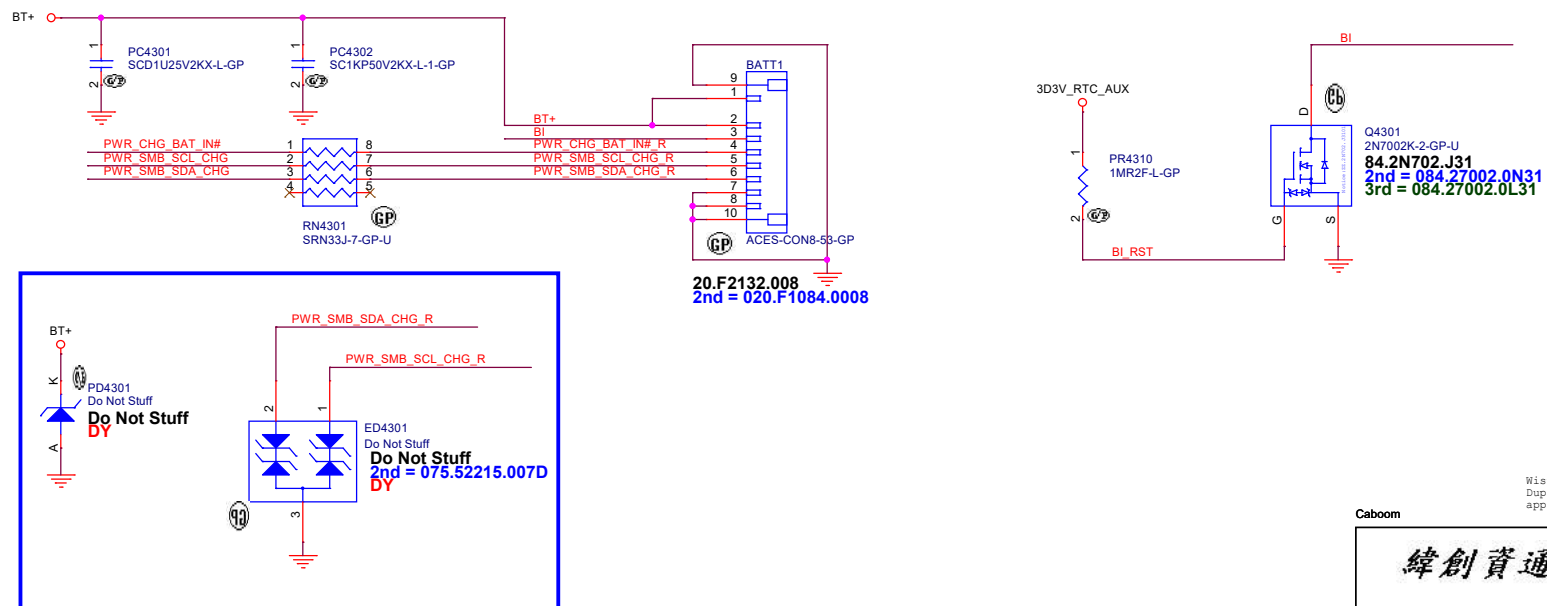
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Title INT IO (TYPEC DC-DC)		
Size A3	Document Number Milgauss_TL	Rev 1
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Annie Solution



Battery Connector

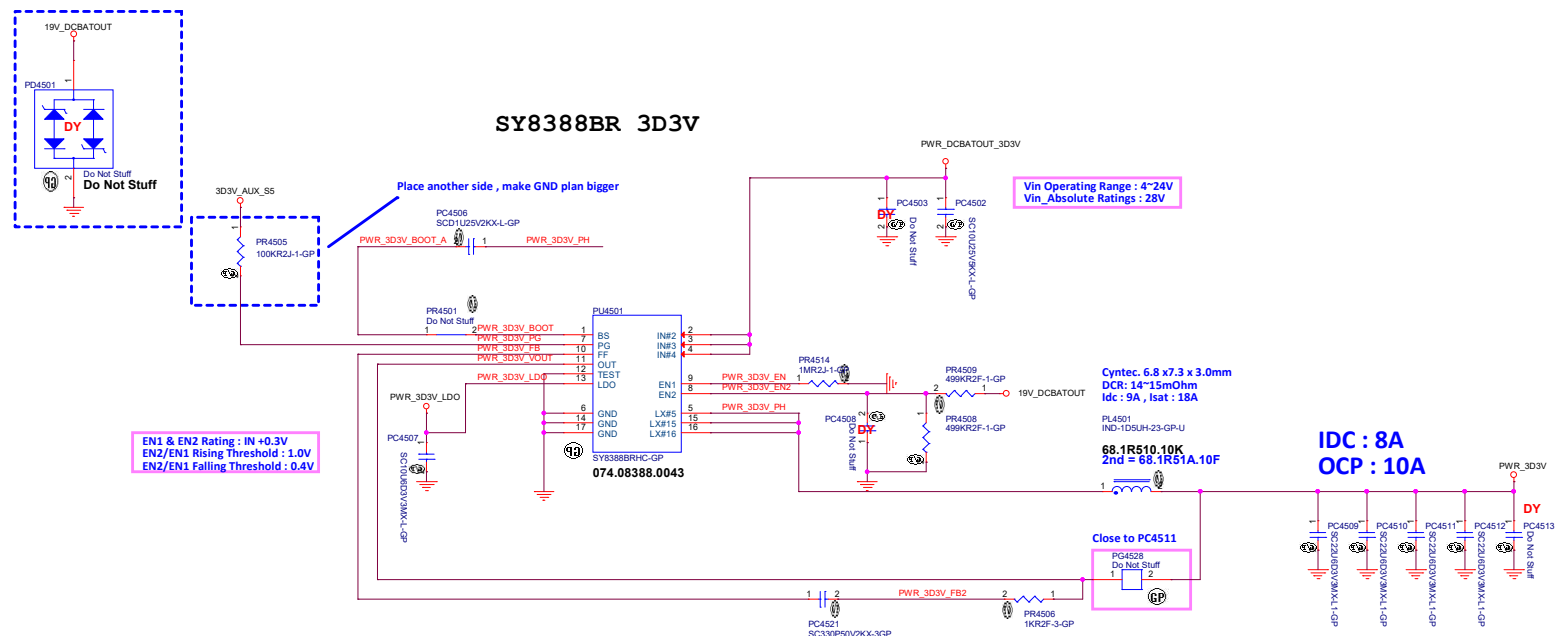
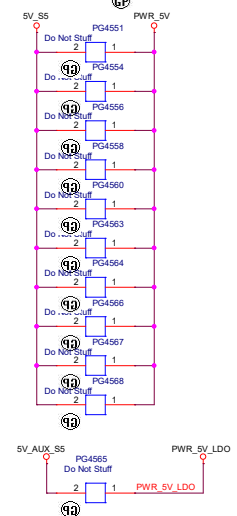
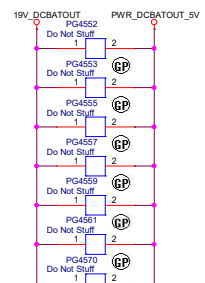
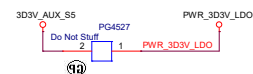
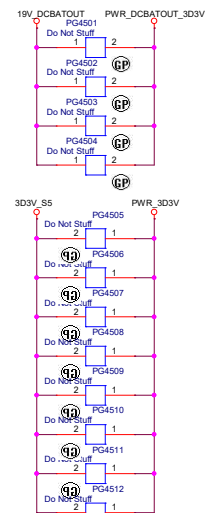


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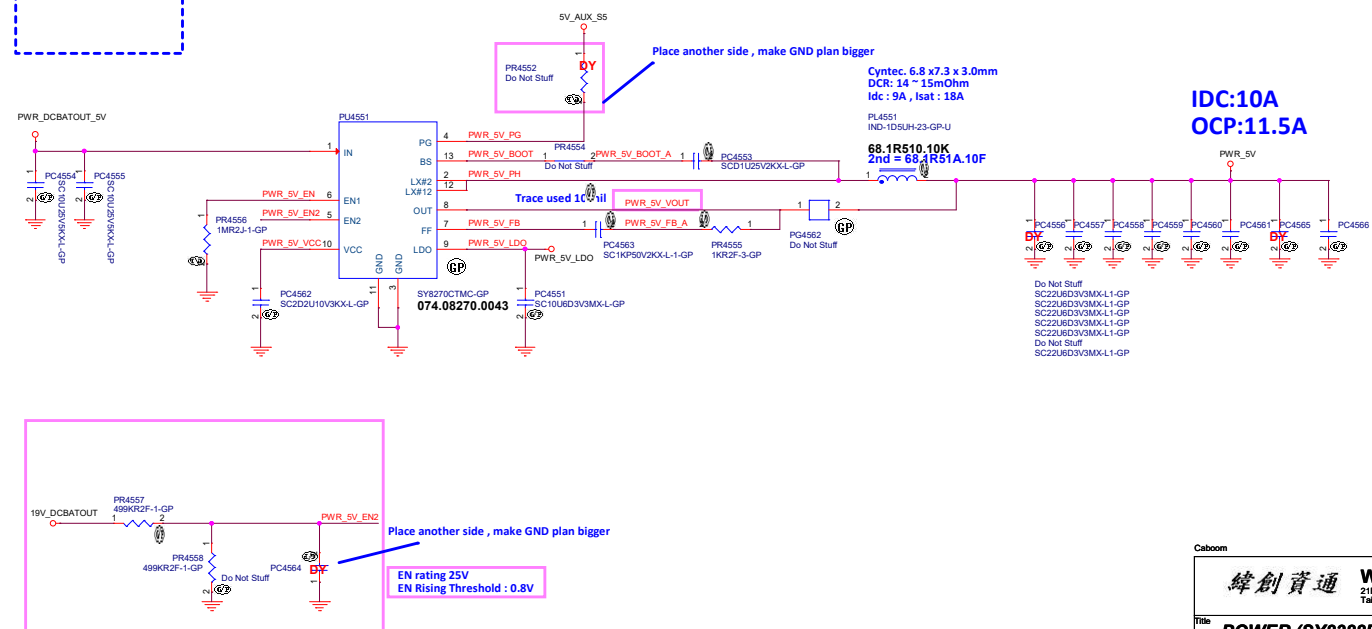
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Title			
INT IO (DC/BATT Conn)			
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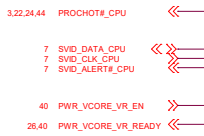
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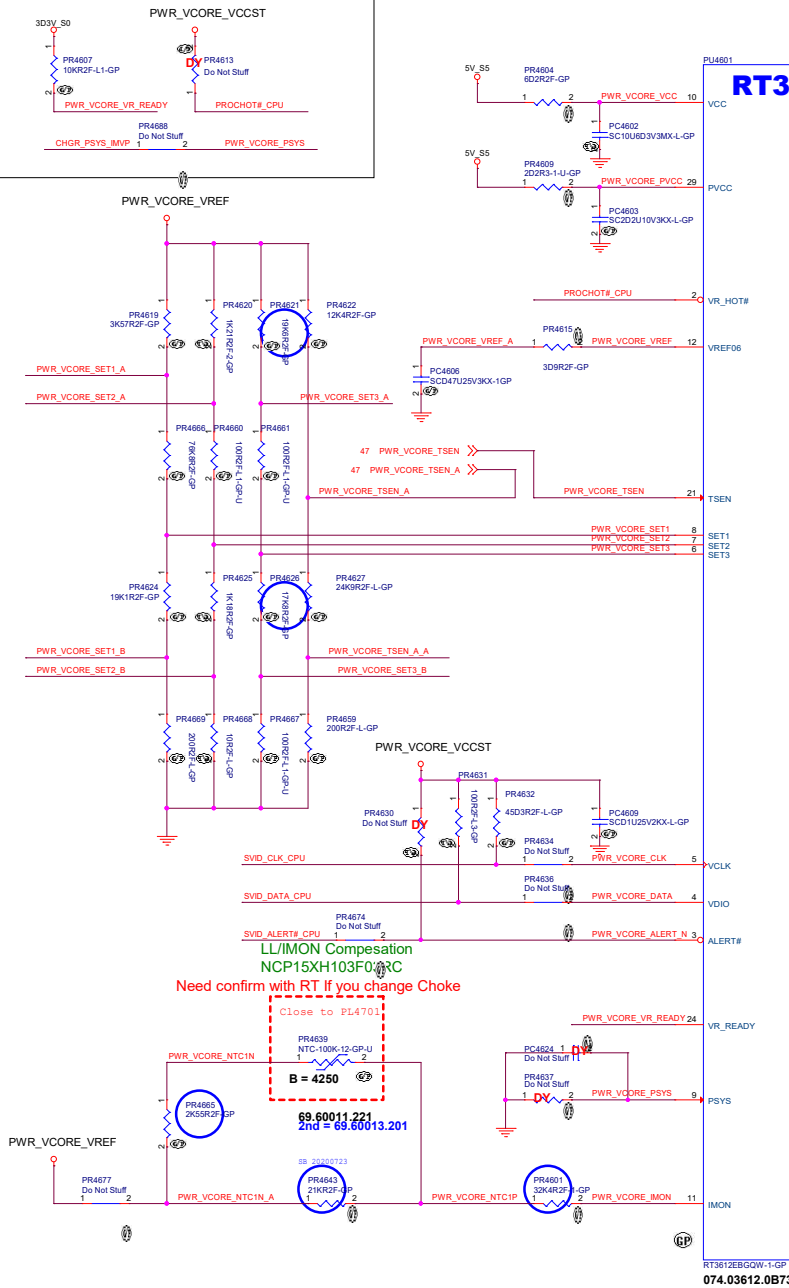
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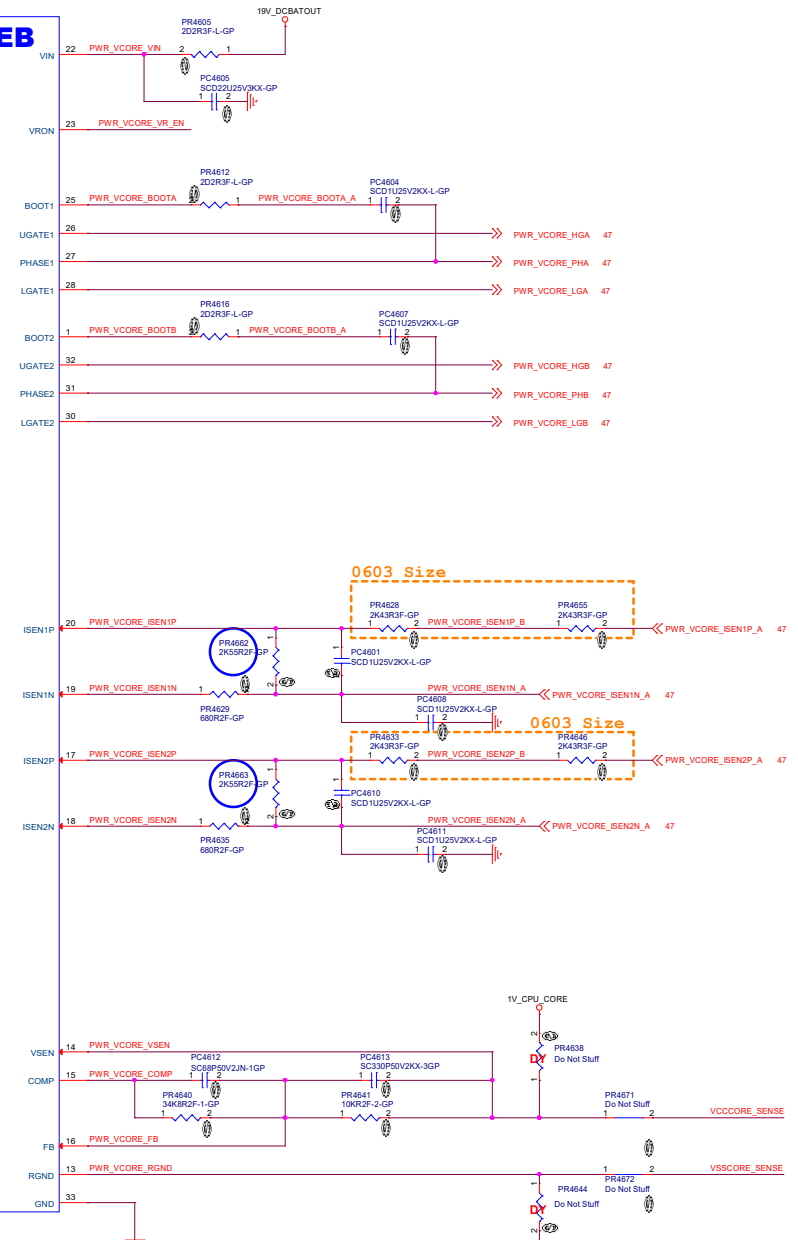
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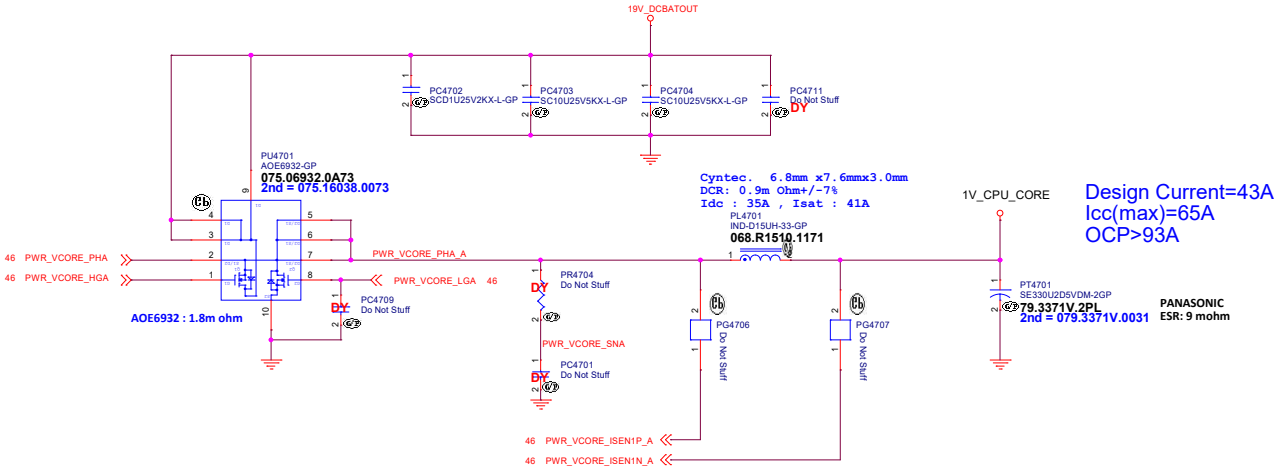
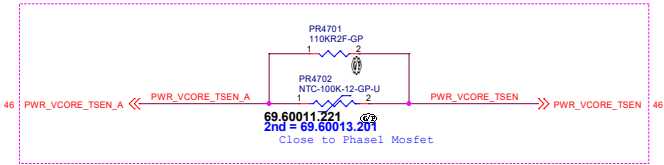


Reserve for Power test

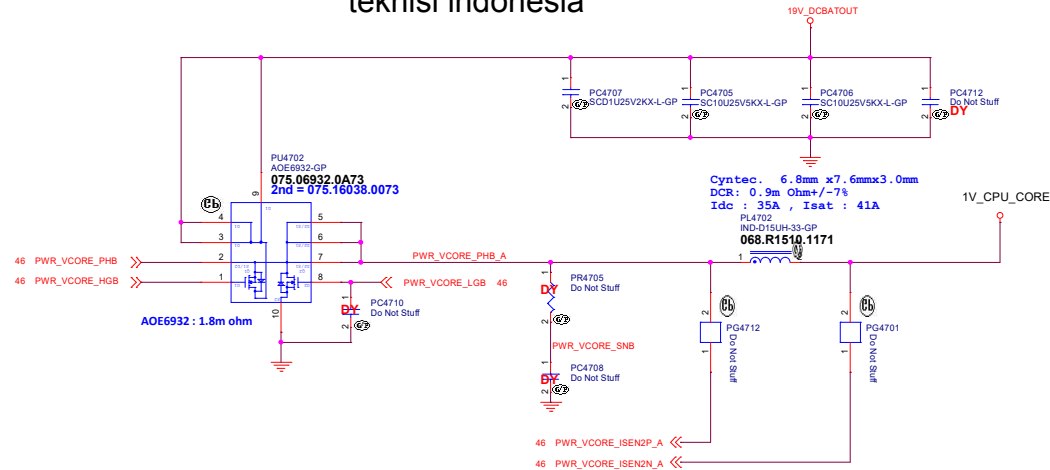


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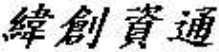
teknisi indonesia



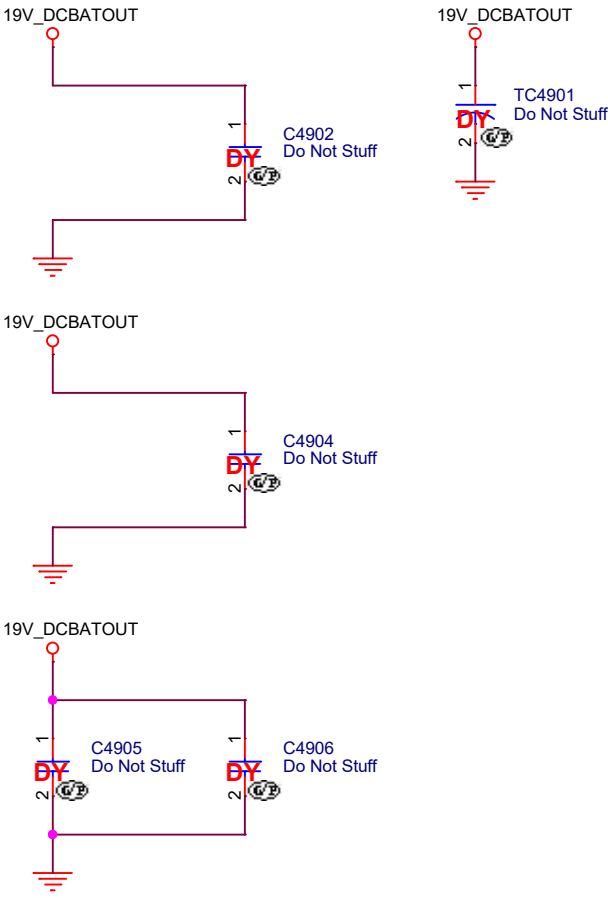
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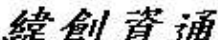
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Low Noise MLCC

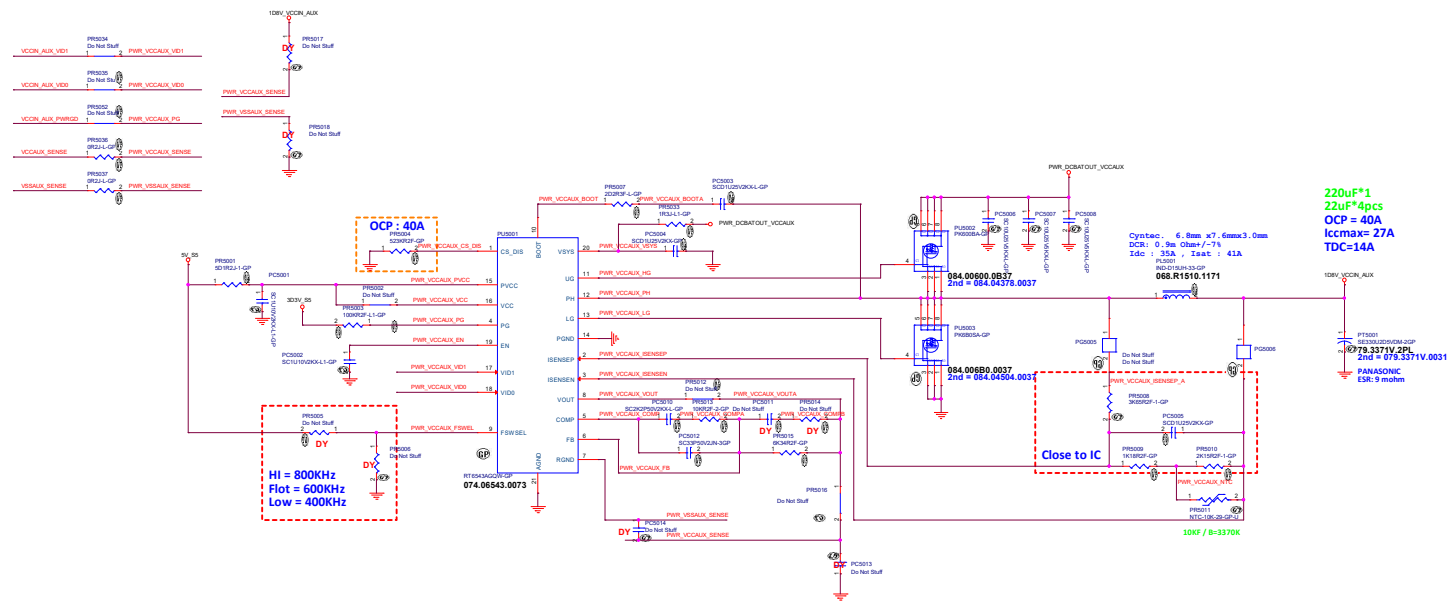


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Title			
POWER (EE Acoustic Noise)			
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53	PWR_VCCAUX_EN	»
40	VCCIN_AUX_PWRRGO	«
22	VCCIN_AUX_VID1	»
22	VCCIN_AUX_VID0	»
22	VCCAUX_SENSE	«
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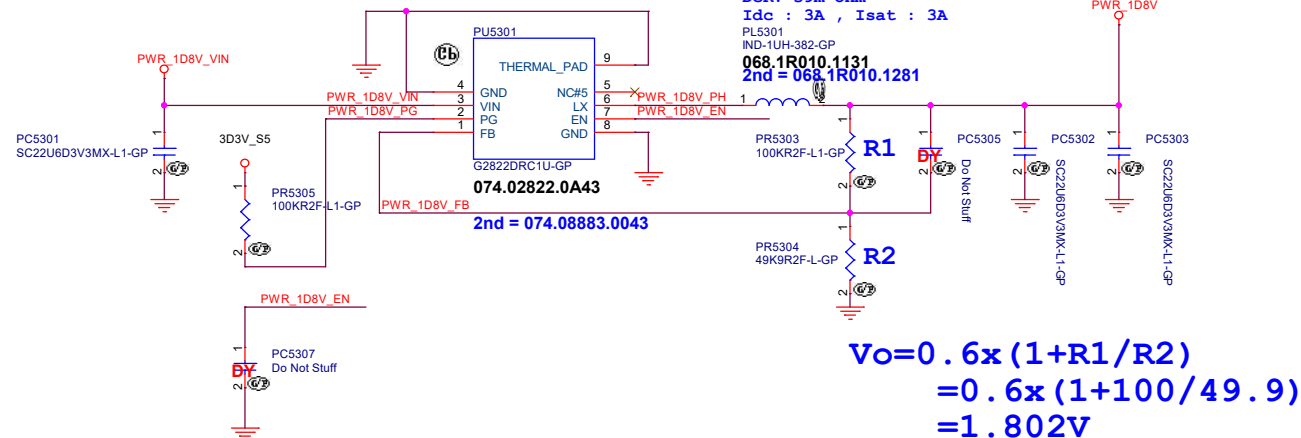
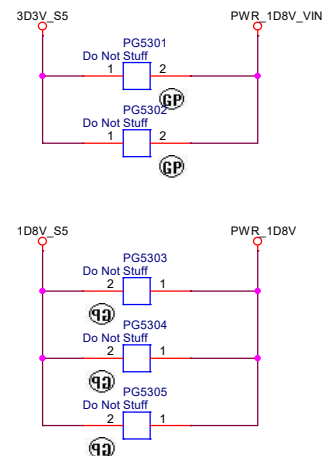
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40 PWR_1D8V_EN

50 PWR_VCCAUX_EN

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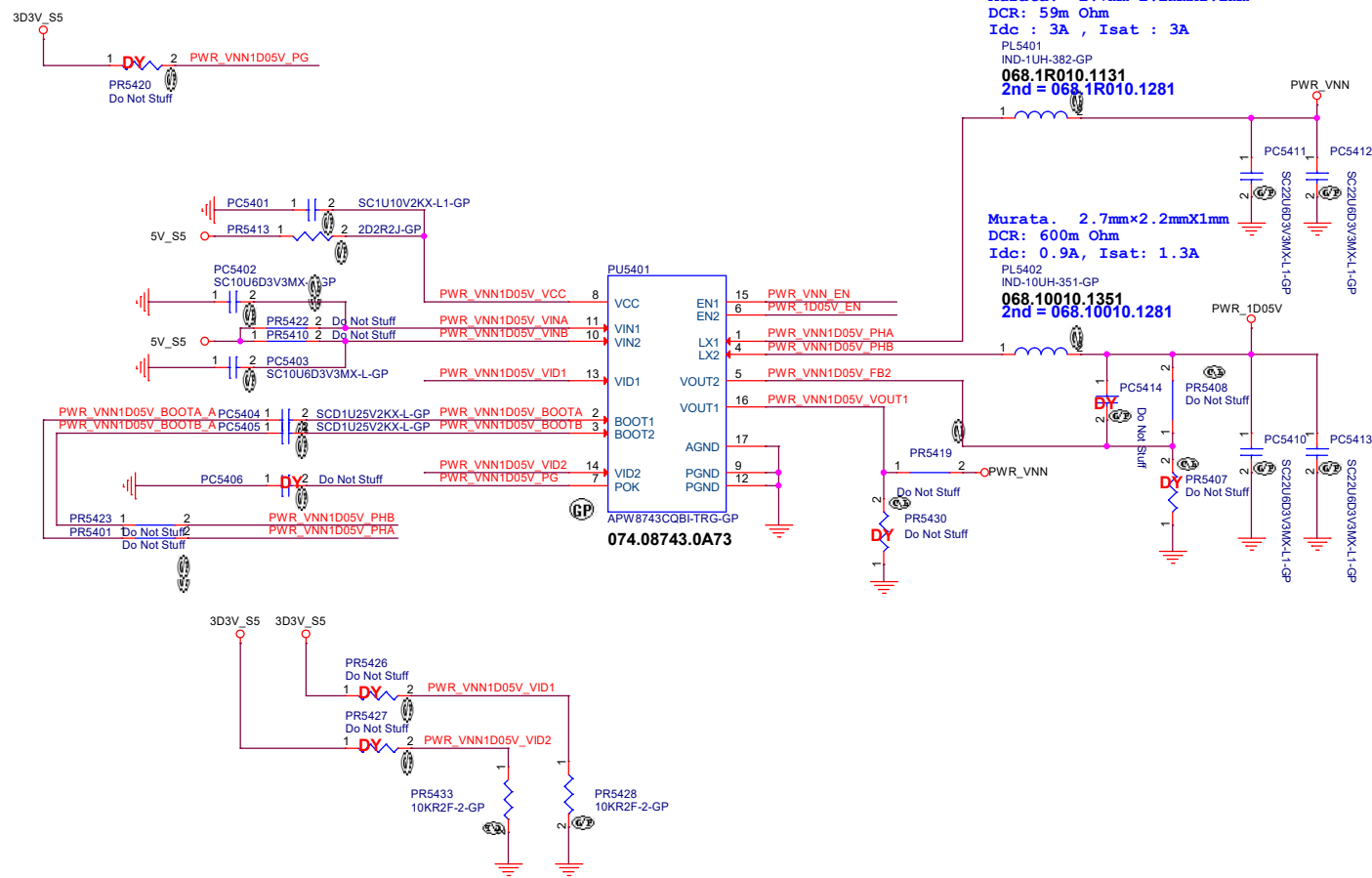
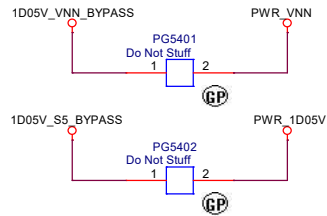
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Power (G2822_1D8V)	
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VCCIN_AUX_PWRGD
PH on EE Side

- 40 PWR_VNN_EN >> VOUT1
- 40 PWR_1D05V_EN >> VOUT2
- 40 PWR_VNN1D05V_VID1 >>
- 40 PWR_VNN1D05V_VID2 >>

OFFPAGE-GAP



VNN_BYPASS VID Table

VID1	Voltage(APW8743C)	Voltage(APW8743D)	Voltage(APW8743E)	Slew Rate
0	1.05V	0.78V	1.05V	10mV/us ~ 20mV/us
1	0.78V	0.7V	0.7V	10mV/us ~ 20mV/us

V1P05A_BYPASS VID Table

VID2	Voltage(APW8743C/D/E)	Slew Rate
0	1.05V	10mV/us ~ 20mV/us
1	0.96V	10mV/us ~ 20mV/us

Main Func = LCD

4 eDP_TX_CPU_N0
4 eDP_TX_CPU_P0
4 eDP_TX_CPU_N1
4 eDP_TX_CPU_P1
4 eDP_TX_CPU_N2
4 eDP_TX_CPU_P2
4 eDP_TX_CPU_N3
4 eDP_TX_CPU_P3

4 eDP_AUX_CPU_N
4 eDP_AUX_CPU_P

4 eDP_HPD_CPU

4 eDP_VDDEN_CPU
4 eDP_BKLTCTL_CPU

24 BLON_OUT

16 CCD_USB20_N
16 CCD_USB20_P

20 CPU_I2C_SDA_TS
20 CPU_I2C_SCL_TS

19 DMIC1_SCL_CPU
19 DMIC1_SDA_CPU
19 DMIC2_SCL_CPU
19 DMIC2_SDA_CPU

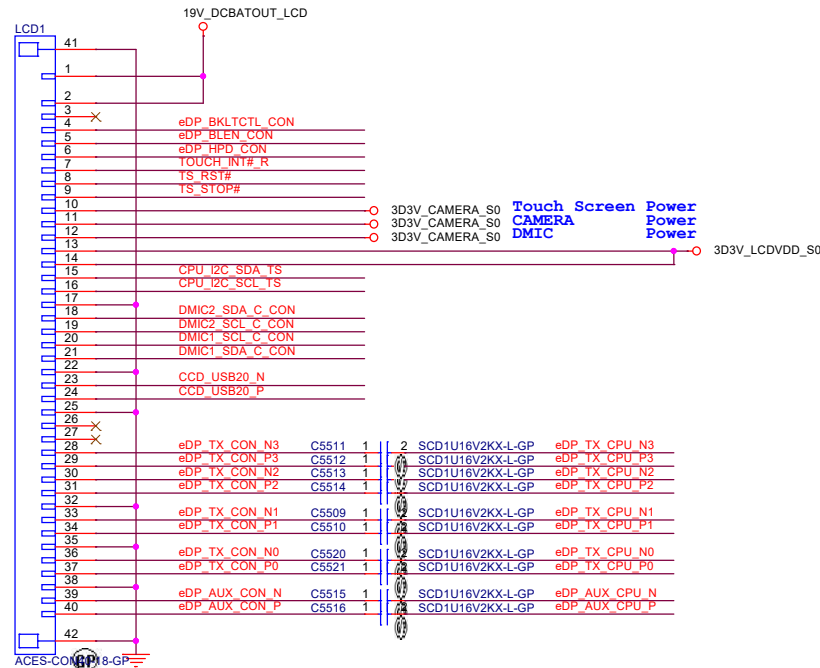
24 TS_RST#

3 TOUCH_INT#

89 eDP_BKLTCTL_CON
89 eDP_BLEN_CON
89 eDP_HPD_CON

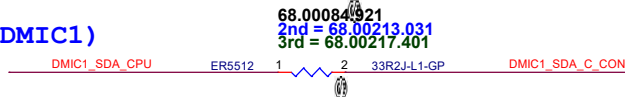
89 DMIC1_SCL_C_CON
89 DMIC1_SDA_C_CON

18 TS_STOP#

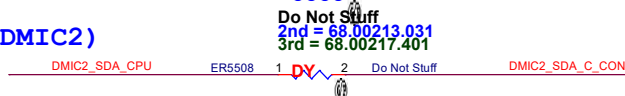


20.K0678.040
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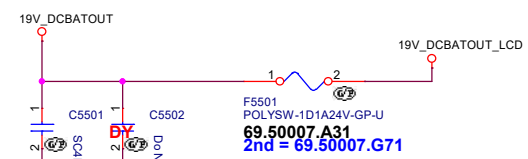
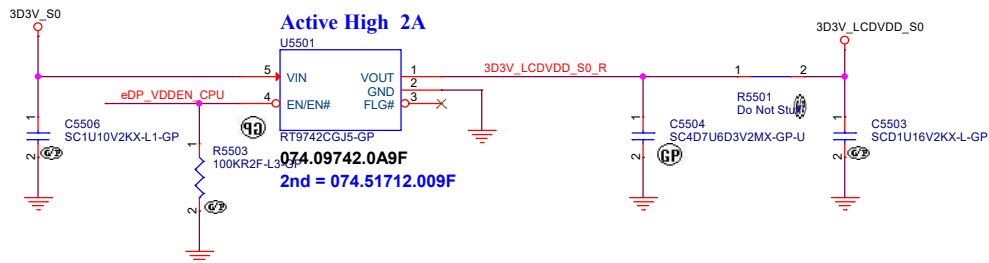
CPU (DMIC1)



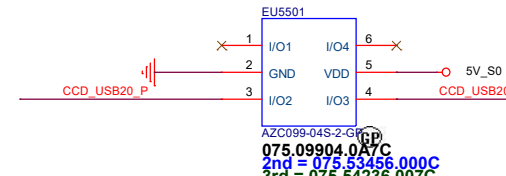
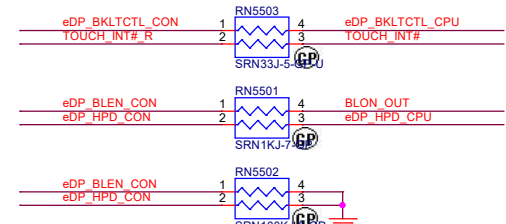
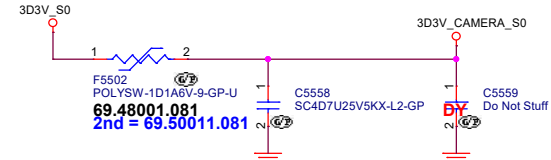
CPU (DMIC2)



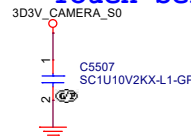
Active High 2A



Camera Power



Touch Screen Power



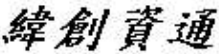
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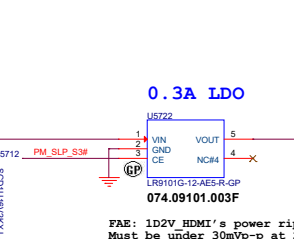
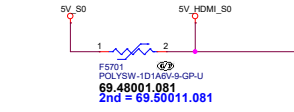
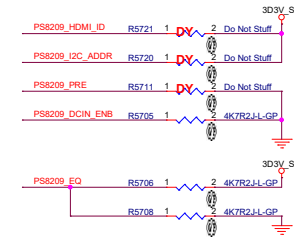
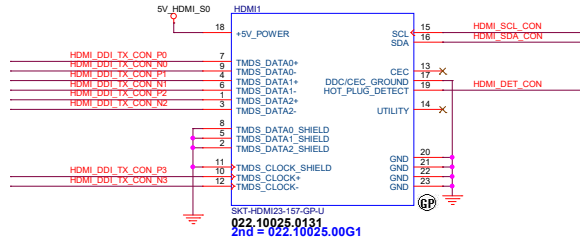
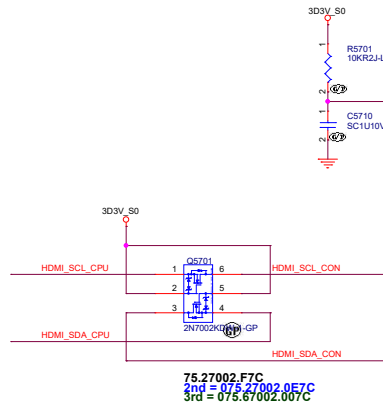
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Title Display (RSVD)			
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Date: Friday, November 06, 2020		Sheet 56 of	106

HDMI 2.0 Repeater

From GPU	To Repeater
HDMI DDI TX P0 C5701 1	2 SCD1U18V2KX4-GP HDMI DDI TX C P0
HDMI DDI TX N0 C5702 1	2 SCD1U18V2KX4-GP HDMI DDI TX C N0
HDMI DDI TX P1 C5703 1	2 SCD1U18V2KX4-GP HDMI DDI TX C P1
HDMI DDI TX N1 C5704 1	2 SCD1U18V2KX4-GP HDMI DDI TX C N1
HDMI DDI TX P2 C5705 1	2 SCD1U18V2KX4-GP HDMI DDI TX C P2
HDMI DDI TX N2 C5706 1	2 SCD1U18V2KX4-GP HDMI DDI TX C N2
HDMI DDI TX P3 C5707 1	2 SCD1U18V2KX4-GP HDMI DDI TX C P3
HDMI DDI TX N3 C5708 1	2 SCD1U18V2KX4-GP HDMI DDI TX C N3

FAB: CPU to PS8209A recommend 6" inch



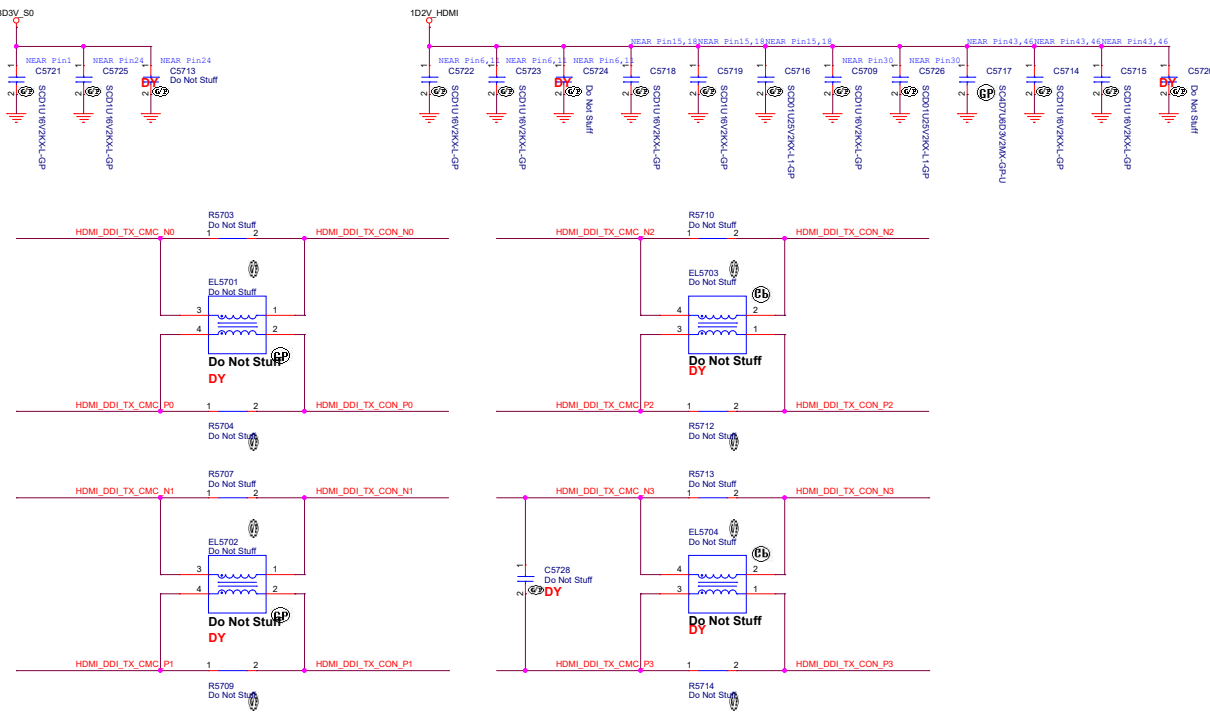
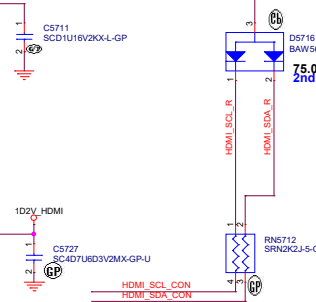
HDMI ID enable : Internal pull down, 3.3V I/O.
I: Default, HDMI ID enable.
H: HDMI ID Disable.

I2C Slave address selection :
Internal pull down, 3.3V I/O.
I: Default, Slave address : 0x10-0x2F.
H: Alternative slave address 0x90-0x9F, 0x00-0x0F

Output pre-emphasis setting : Internal pull up, 3.3V I/O.
I: Pre-emphasis +2.5dB.
H: Default, No pre-emphasis

DC coupling enable; Internal pull up, 3.3V I/O.
I: DC coupling input.
H: Default, AC coupling input

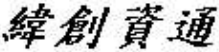
Receiver equalization setting :
Internal pull up, 3.3V I/O.
I: Compensation for channel loss up to 13db
H: Default, compensation for channel loss up to 17db
M: Compensation for channel loss up to 11db



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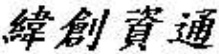
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Title Display (RSVD)			
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Title Display (RSVD)			
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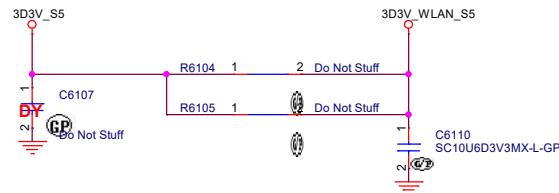
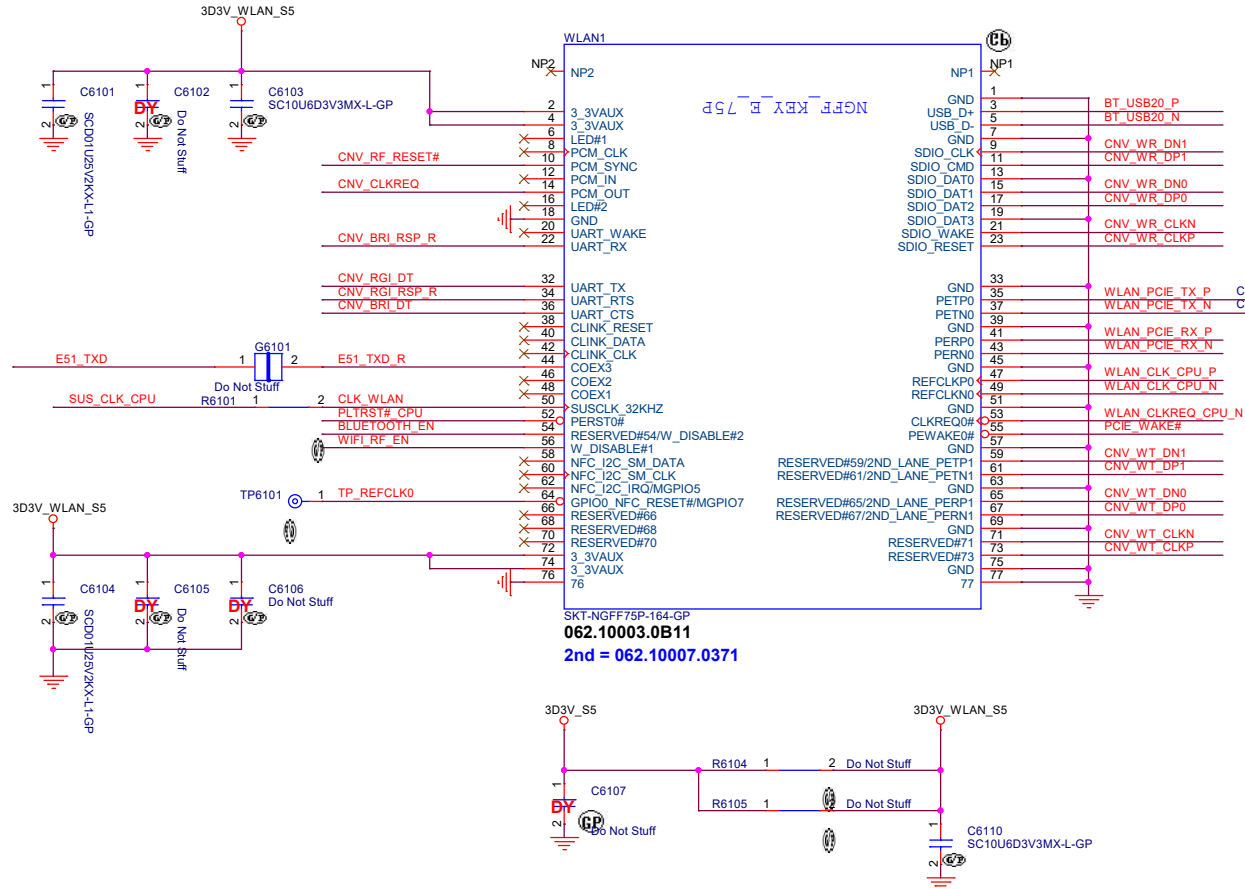
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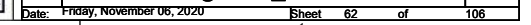
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>INT IO (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Milgauss_TL</div>	Rev <div>1</div>
Date <div>Friday, November 06, 2020</div>		Sheet <div>60</div> of <div>106</div>

Mini Card Connector (802.11a/b/g/n)



Title				INT IO (WLAN M.2)			
Size A3	Document Number					Rev	
	Milgauss_TL					1	
Date:	Friday, November 06, 2020			Sheet	61	of	106

Mini Card Connector (PCIe Gen3/SATA Gen3)

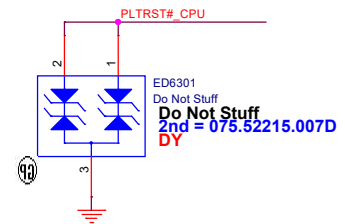
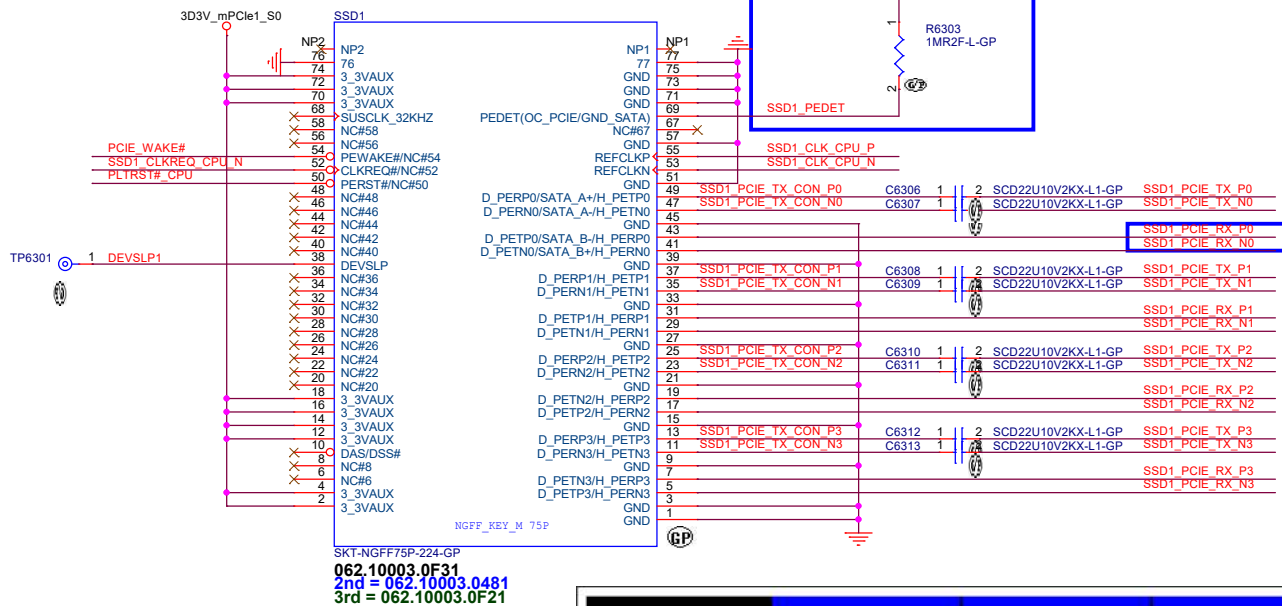
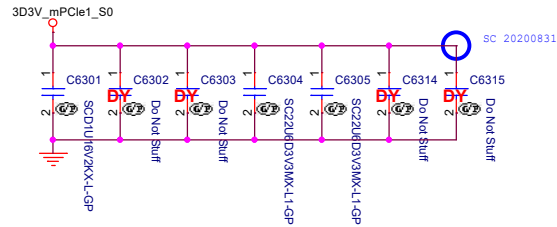
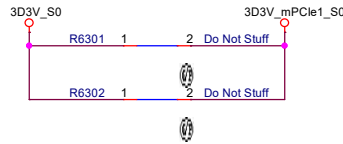


SSID = mPCIe

Mini Card Connector(PCIe Gen4)

17,61,62,89 PCIE_WAKE# <<>>
18 SSD1_CLKREQ_CPU_N <<>>
71,72,89,91 PLTRST#_CPU <<>>

18 SSD1_CLK_CPU_P <<>>
18 SSD1_CLK_CPU_N <<>>
16 SSD1_PCIE_TX_P0 <<>>
16 SSD1_PCIE_TX_N0 <<>>
16 SSD1_PCIE_RX_P0 <<>>
16 SSD1_PCIE_RX_N0 <<>>
16 SSD1_PCIE_TX_P1 <<>>
16 SSD1_PCIE_TX_N1 <<>>
16 SSD1_PCIE_RX_P1 <<>>
16 SSD1_PCIE_RX_N1 <<>>
16 SSD1_PCIE_TX_P2 <<>>
16 SSD1_PCIE_TX_N2 <<>>
16 SSD1_PCIE_RX_P2 <<>>
16 SSD1_PCIE_RX_N2 <<>>
16 SSD1_PCIE_TX_P3 <<>>
16 SSD1_PCIE_TX_N3 <<>>
16 SSD1_PCIE_RX_P3 <<>>
16 SSD1_PCIE_RX_N3 <<>>



SKT-NGFF75P-224-GP
062.10003.0F31
2nd = 062.10003.0481
3rd = 062.10003.0F21

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12
Logical Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1	0	1	0	1
	2x2 LR	1	0	1	0	1	0	1	0	1	0	1	0
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0
Assigned Root Ports	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	2x2 LR	RP3		RP1		RP7		RP5		RP11		RP9	
	1x2+2x1	RP1		RP3		RP4		RP5		RP7		RP8	
	2x1+1x2	RP4		RP3		RP1		RP8		RP7		RP5	
Assigned Root Ports	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

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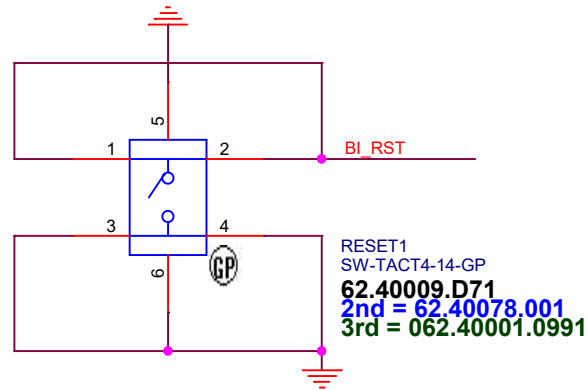
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Title		INT IO (SSD1 M.2)	
Size A3	Document Number	Milgauss_TL	
Date: Friday, November 08, 2020	Sheet	63	of 106

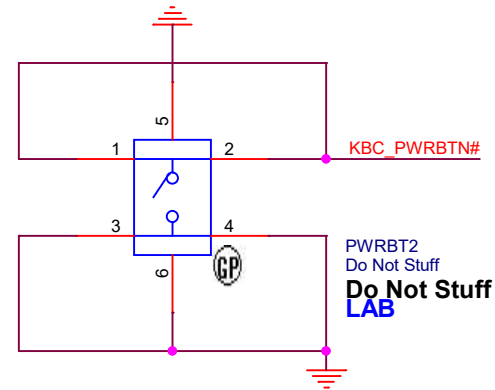
43,89 BI_RST
24,66,89 KBC_PWRBTN#



Battery Reset



Power Button



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Title

LED / Button / Power Button

Size
A4

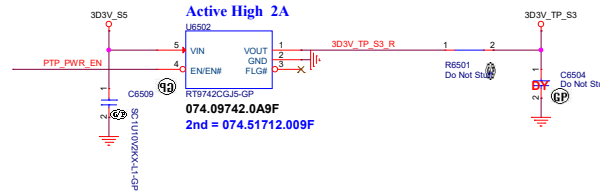
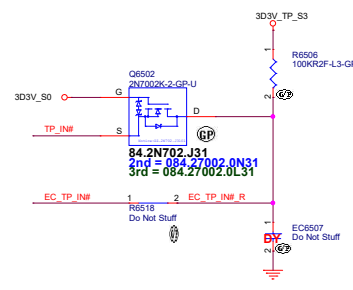
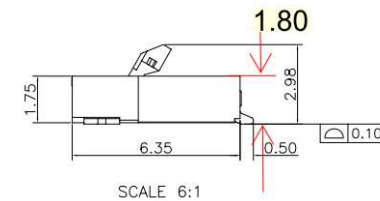
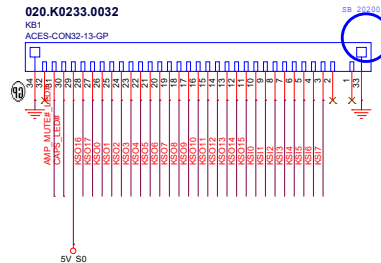
Document Number

Milgauss_TL

Rev
1

Date: Friday, November 06, 2020

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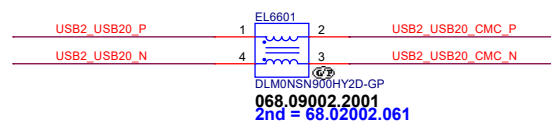
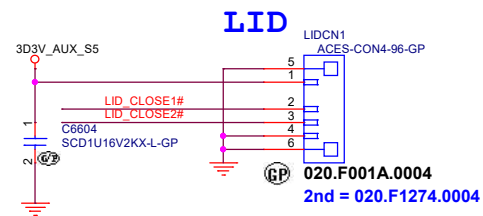
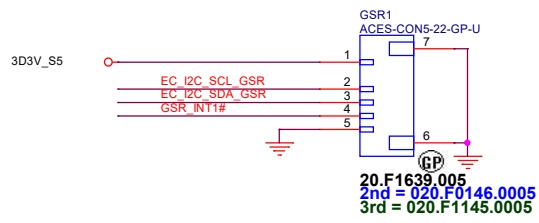
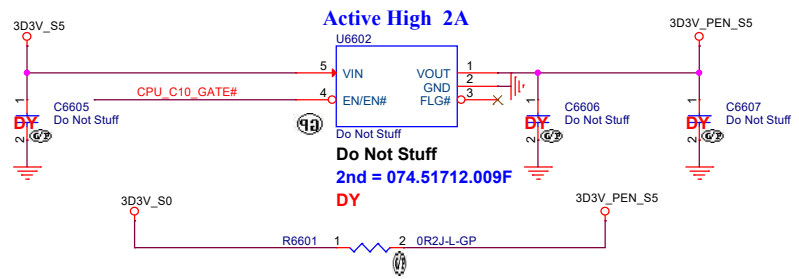
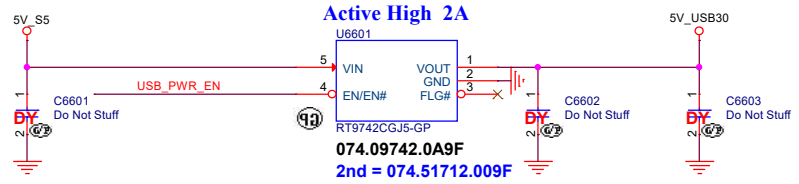
KBBL1
ACES.COM 83

A diagram of a vertical pipe section. A horizontal line near the bottom is labeled "CARBON DOWN". Below this line, a dimension of "32'" is indicated on the left side, spanning the width of the pipe section.

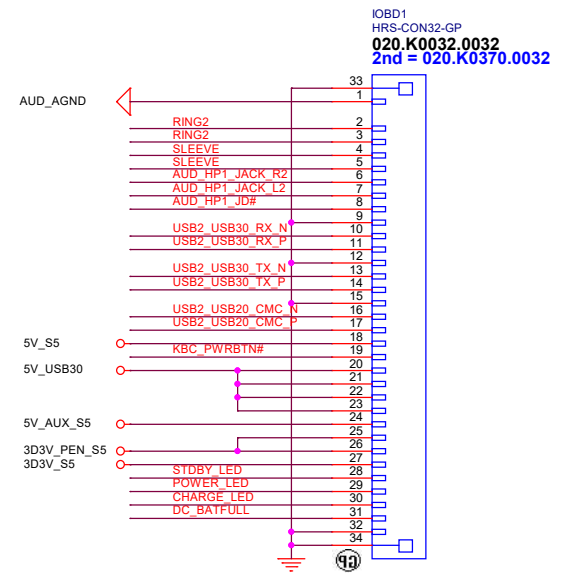
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SSID = User.Interface

- 27.89 RING2
- 27.89 SLEEVE
- 27.89 AUD_HP1_JACK_R2
- 27.89 AUD_HP1_JACK_L2
- 27 AUD_HP1_JD#
- 24 USB_PWR_EN
- 16 USB2_USB30_RX_N
- 16 USB2_USB30_RX_P
- 16 USB2_USB30_TX_N
- 16 USB2_USB30_TX_P
- 16.89 USB2_USB20_N
- 16.89 USB2_USB20_P
- 17.40 CPU_C10_GATE#
- 24.64.89 KBC_PWRBTN#
- 24.89 STDBY_LED
- 24.89 POWER_LED
- 24.89 CHARGE_LED
- 24.89 DC_BATFULL
- 24.89 LID_CLOSE1#
- 24.89 LID_CLOSE2#
- 24.70 GSR_INT1#
- 24.70 EC_I2C_SDA_GSR
- 24.70 EC_I2C_SCL_GSR



IOBD1:
5V_USB30 for USB 3.0
5V_AUX_S5 & 5V_S5 for LED
3D3V_PEN_S5 for PEN
3D3V_S5 for USB3.0 ReDriver



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IO Board Conn (USB3.0)	
Title Size A3 Date: Friday, November 08, 2020	Document Number Milgauss_TL Sheet 66 of 106
Rev 1	Rev 1

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Title <div>Sensor (RSVD)</div>		
Size <div>A4</div>	Document Number <div>Milgauss_TL</div>	Rev <div>1</div>
Date: Friday, November 06, 2020		Sheet 67 of 106



B

A

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Debug (ESPI Conn)

Milgauss_TL

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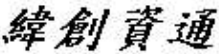
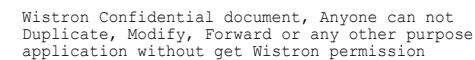
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sensor (RSVD)			
Size A4	Document Number Milgauss_TL		Rev 1
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Diagram illustrating the use of arrows to indicate direction or flow:

- A single left-pointing arrow (\leftarrow) is shown above a horizontal line.
- A pair of opposing arrows (\longleftrightarrow) is shown below a horizontal line.

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.

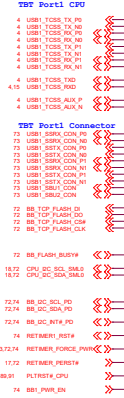
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



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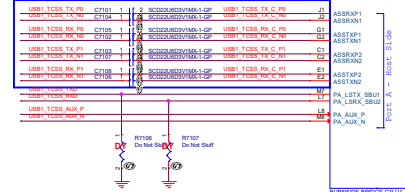
Title				Sensor (G-sensor)			
Size A4	Document Number					Rev	
	Milgauss_TL					1	
Date:	Friday, November 06, 2020			Sheet	70	of	106

Figure 26: I²C connection

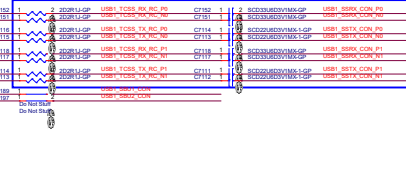


BOM use KI.T3R01.840
U7101 MP use
KI.T3R01.840
2nd: KI.T3R01.840

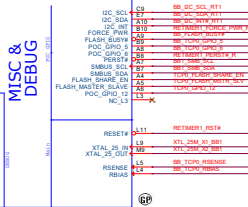
0201 Footprint



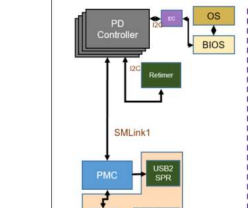
0201 Footprint



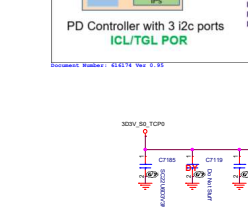
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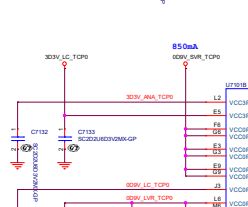
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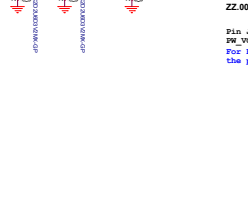
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ZZ.000IC.002



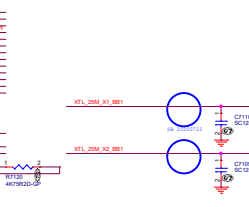
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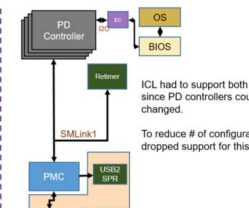
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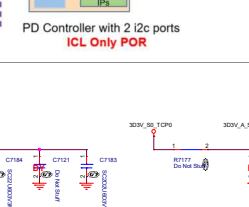
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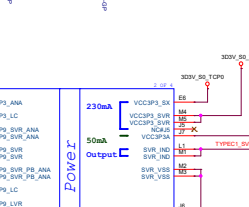
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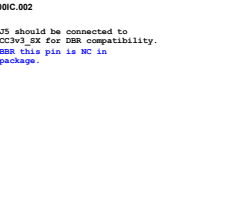
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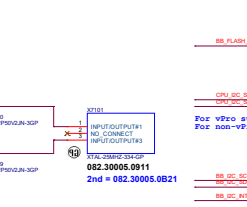
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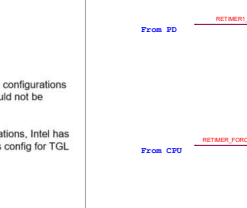
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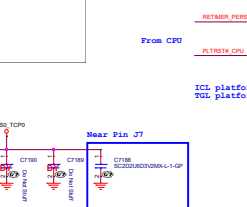
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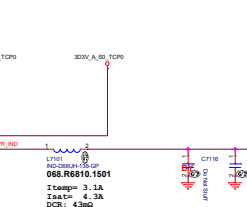
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ZZ.000IC.002



ZZ.000IC.002



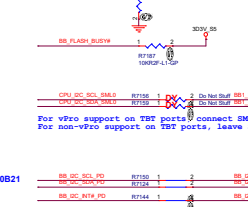
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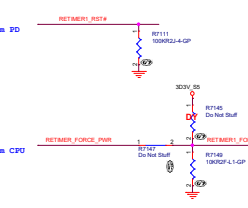
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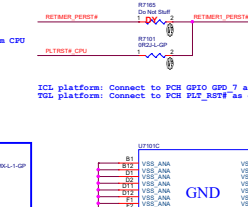
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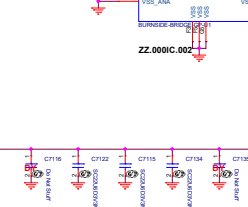
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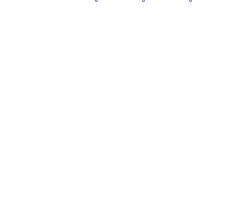
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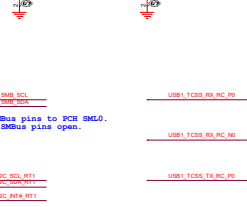
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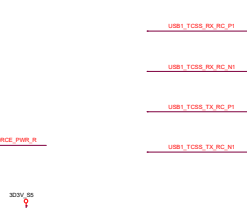
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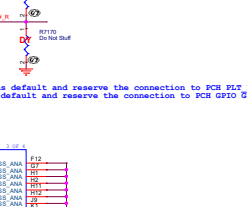
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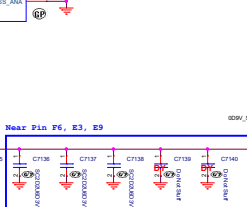
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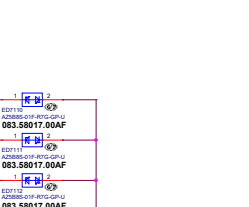
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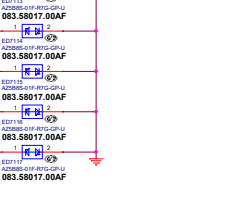
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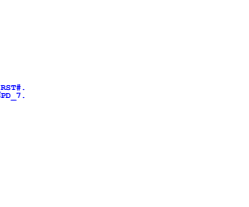
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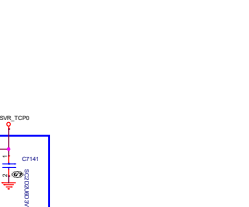
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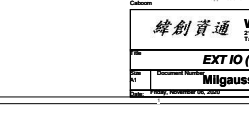
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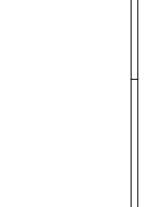
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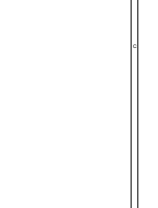
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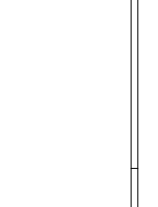
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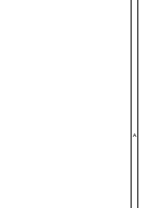
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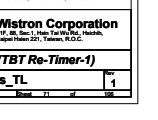
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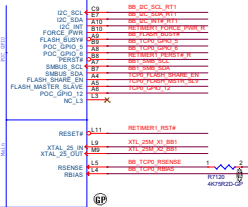
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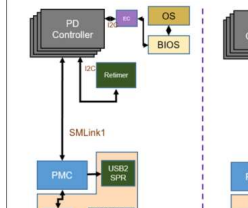
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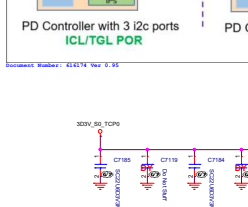
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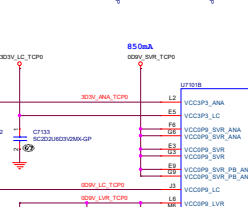
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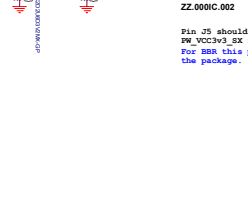
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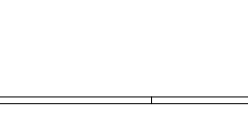
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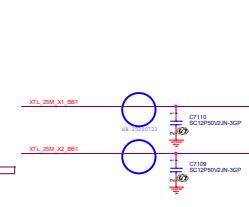
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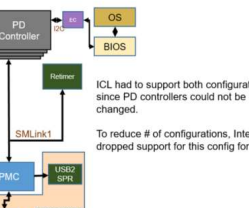
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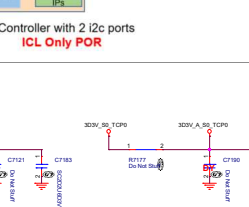
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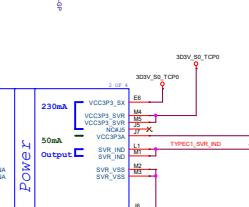
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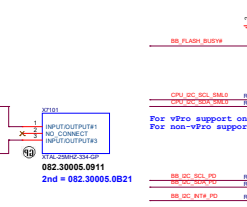
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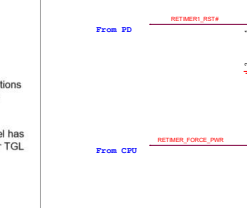
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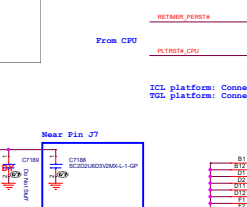
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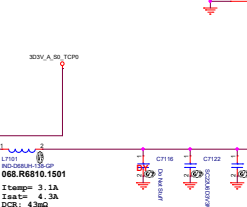
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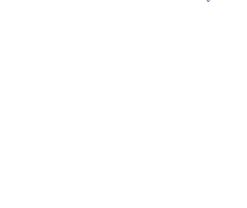
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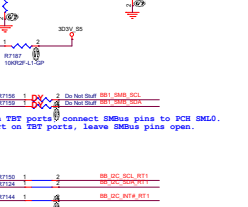
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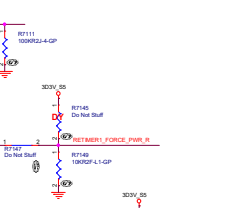
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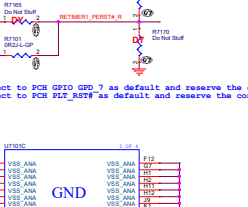
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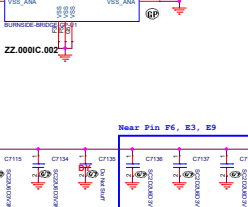
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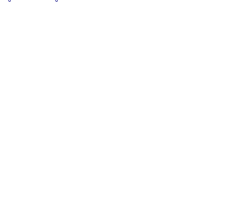
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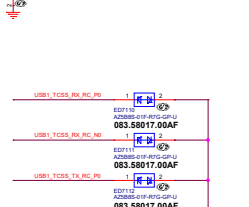
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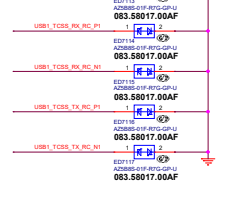
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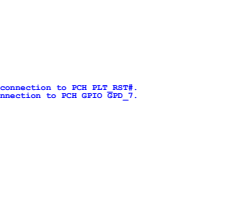
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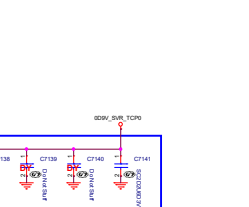
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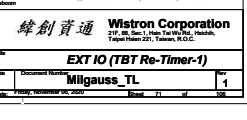
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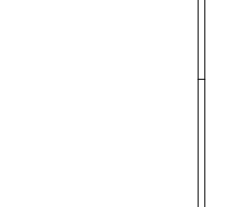
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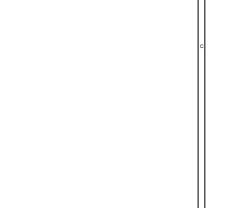
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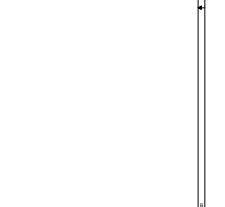
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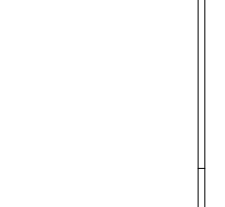
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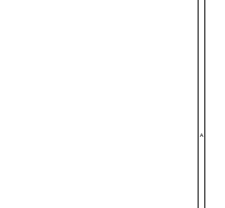
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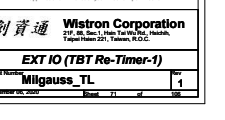
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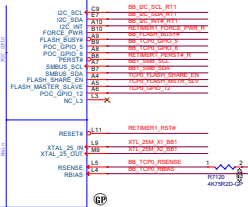
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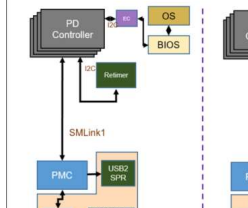
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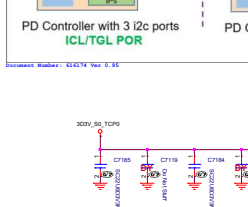
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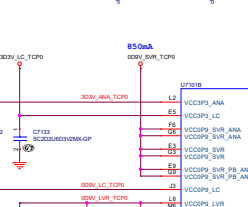
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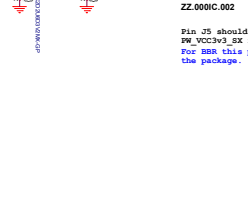
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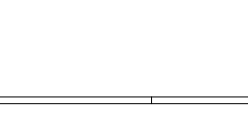
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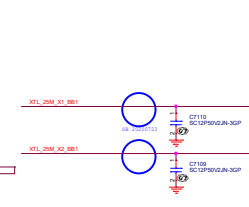
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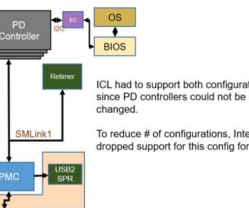
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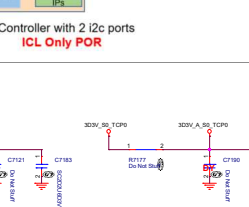
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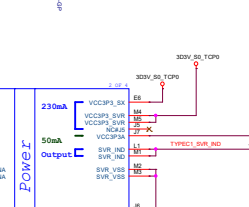
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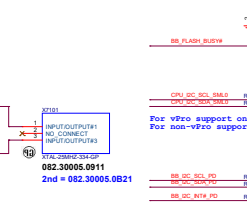
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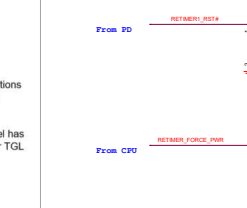
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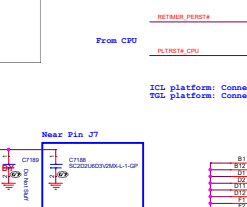
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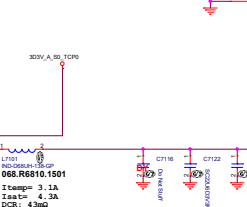
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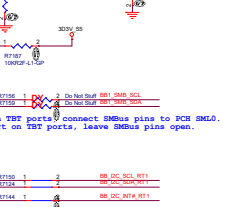
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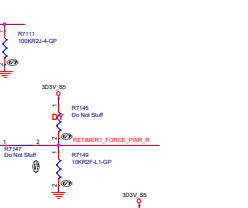
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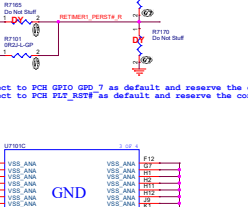
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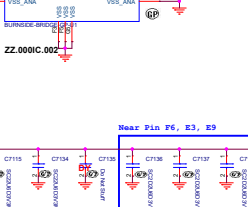
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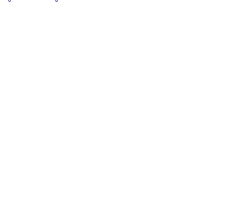
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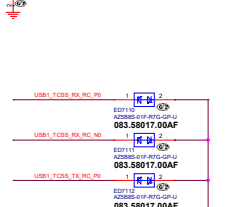
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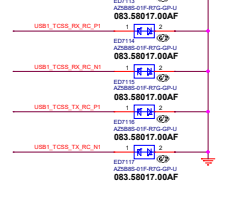
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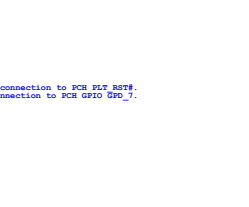
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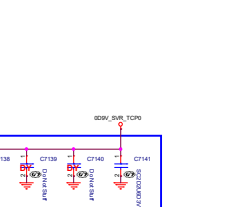
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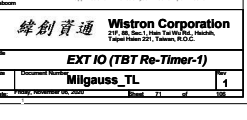
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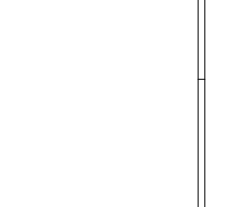
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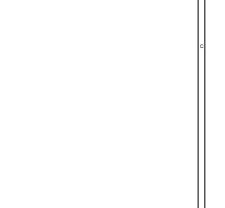
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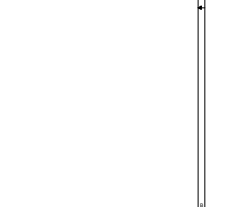
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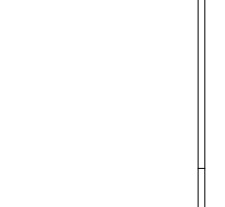
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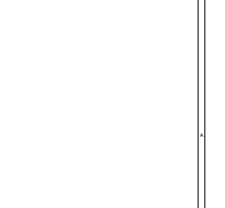
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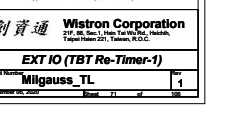
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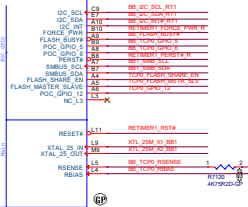
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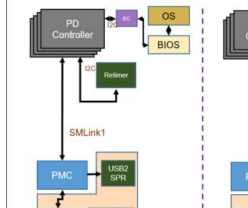
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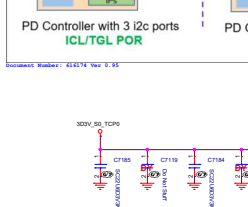
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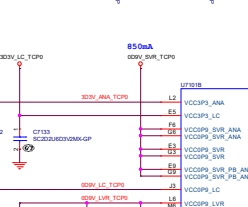
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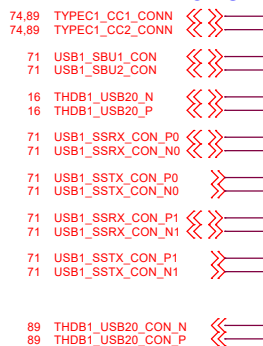
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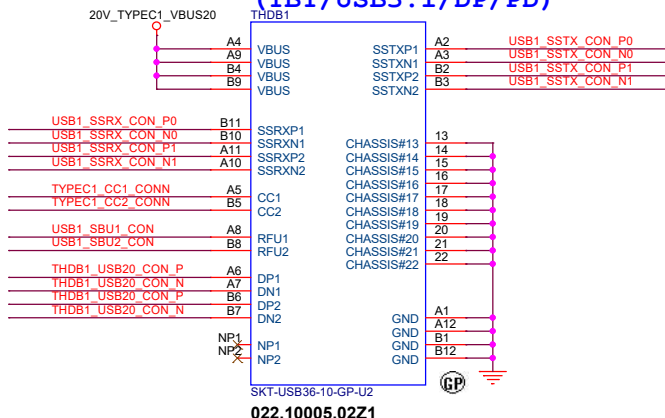
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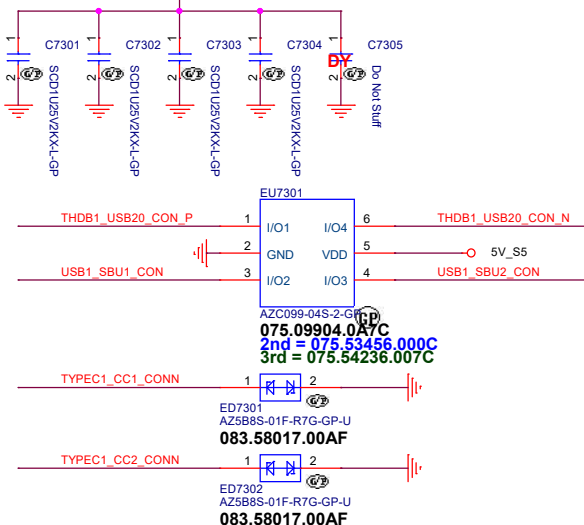
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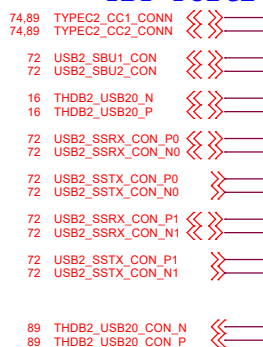
TBT Port1 (TCP0) (TBT/USB3.1/DP/PD)



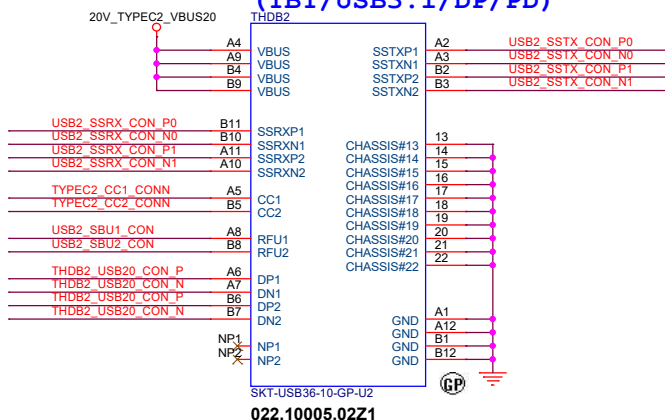
20V_TYPEC1_VBUS20 As close as possible to
USBC connector pins A4/A9/B4/B9



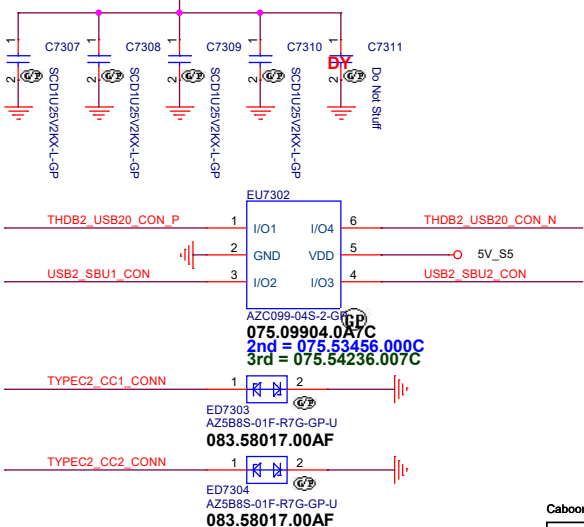
TBT Port2



TBT Port2 (TCP2) (TBT/USB3.1/DP/PD)



20V_TYPEC2_VBUS20 As close as possible to
USBC connector pins A4/A9/B4/B9



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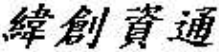
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Size <div>A4</div>	Document Number <div>Milgauss_TL</div>	Rev <div>1</div>
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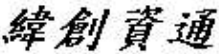
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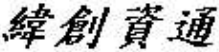
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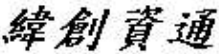
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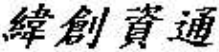
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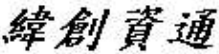
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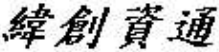
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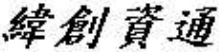
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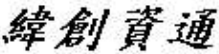
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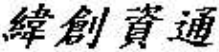
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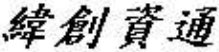
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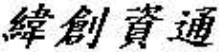
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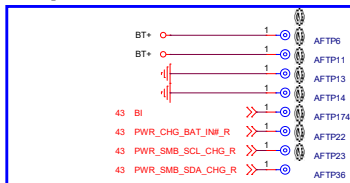
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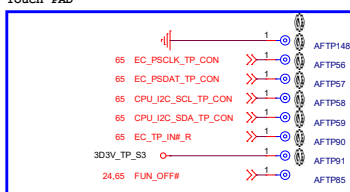
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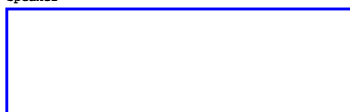
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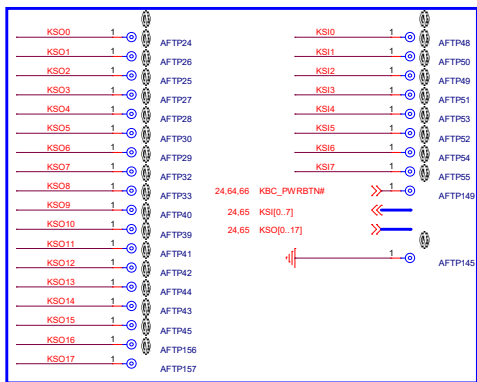
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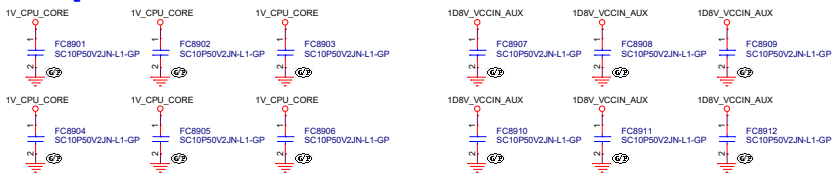
Speaker



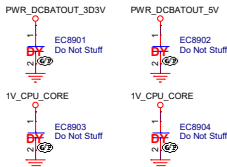
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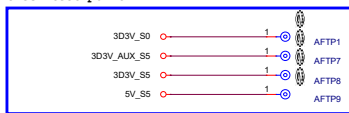
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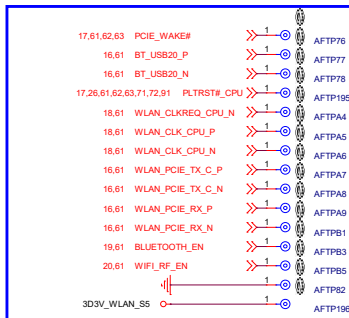
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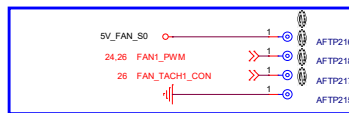
Top side
Check test point



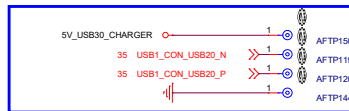
WLAN



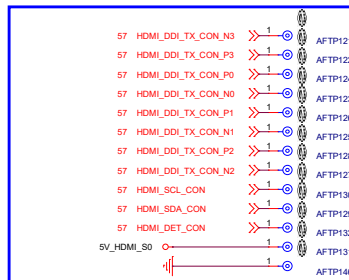
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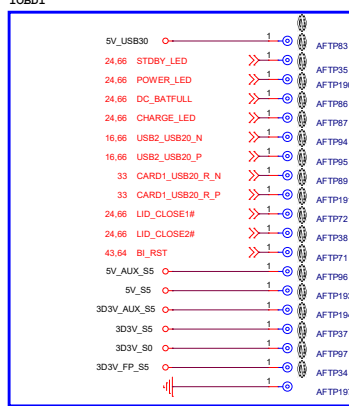
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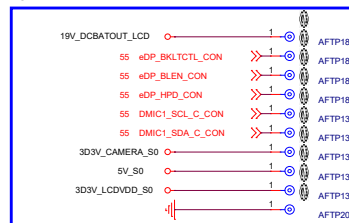
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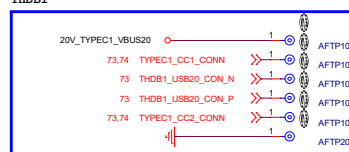
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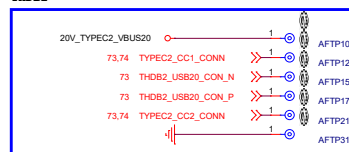
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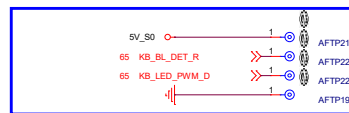
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THDB2



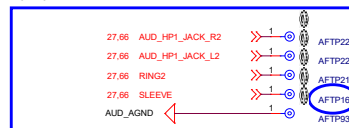
KBBL1



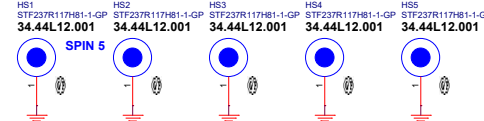
RTC1



AUDIO1



Stand off 1



Screw pad



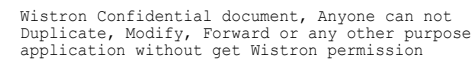
Co-Lay HS1

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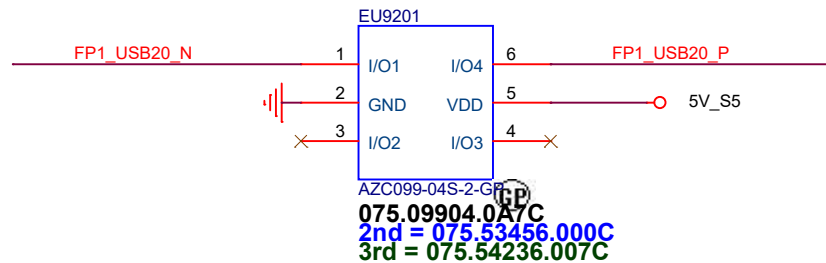
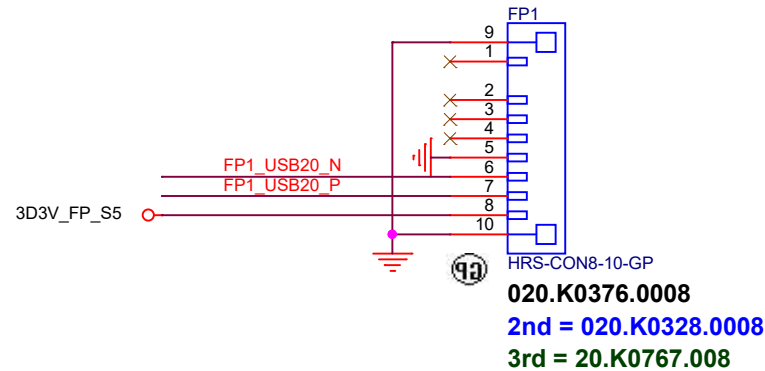
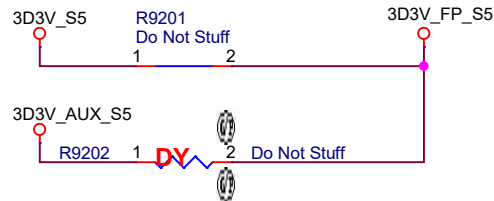
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INT IO (TPM)

number **Milgauss_TL**

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16 FP1_USB20_N
16 FP1_USB20_P



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Taipei Hsien 221, Taiwan, R.O.C.

Title
INT IO (Finger Printer)

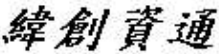
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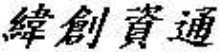
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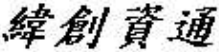
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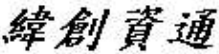
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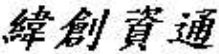
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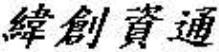
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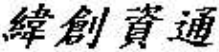
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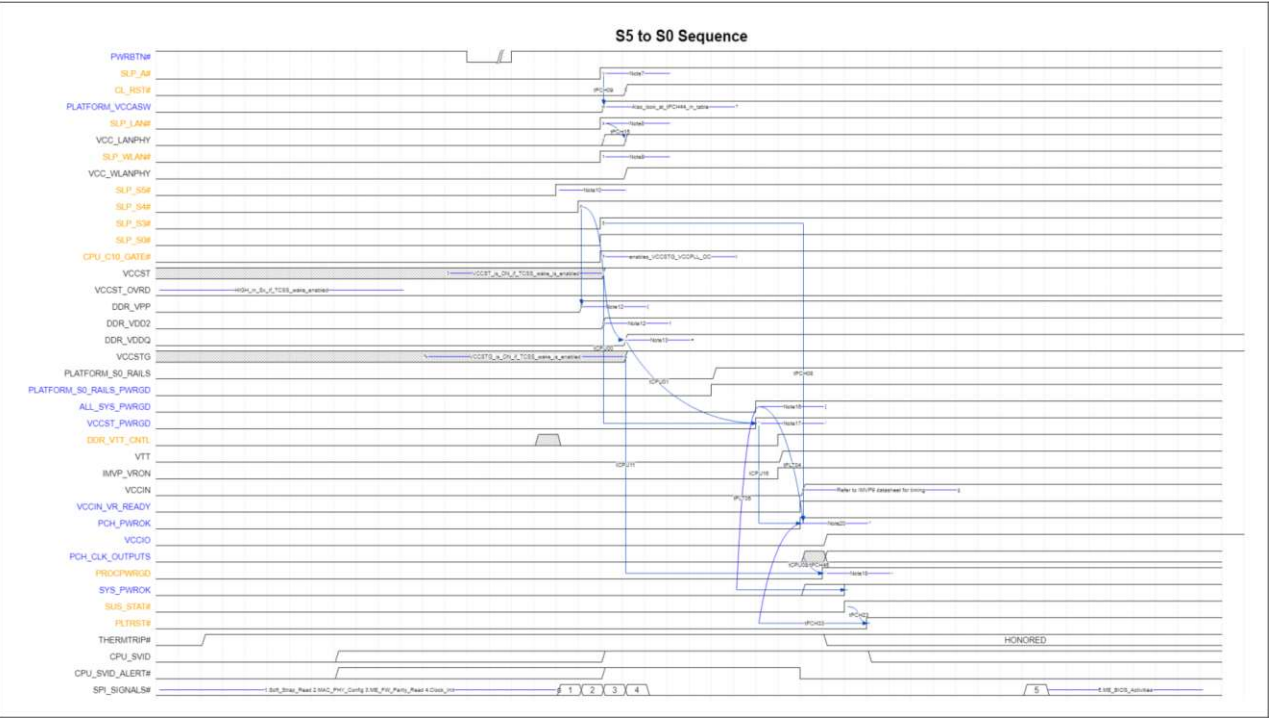
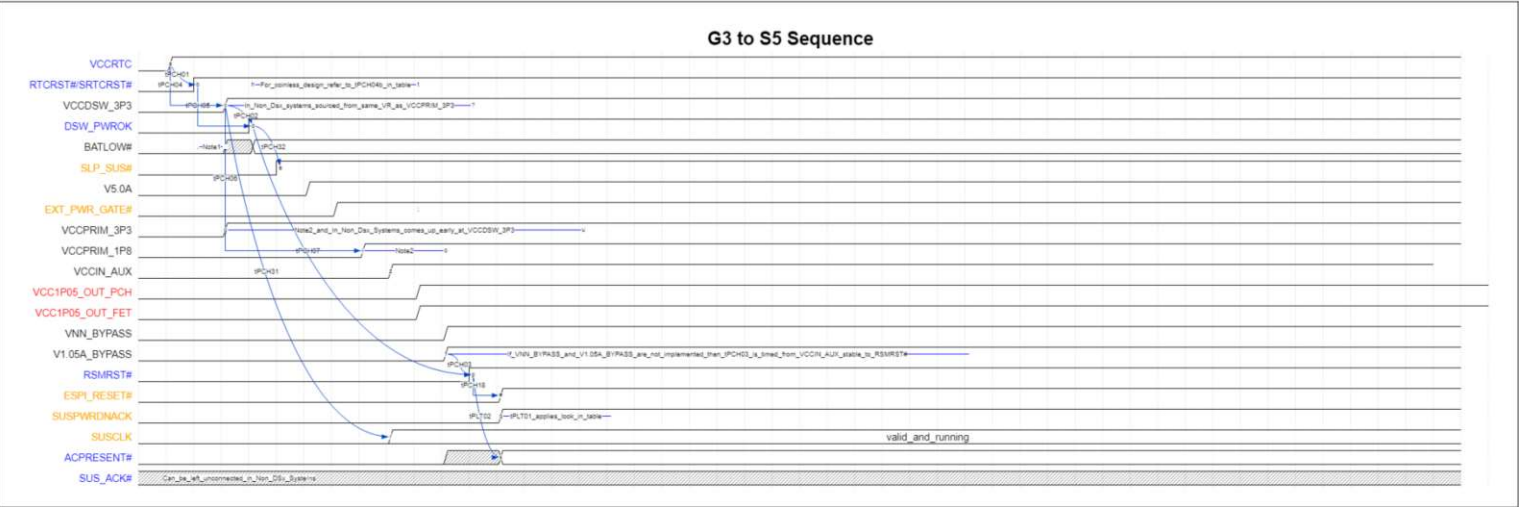
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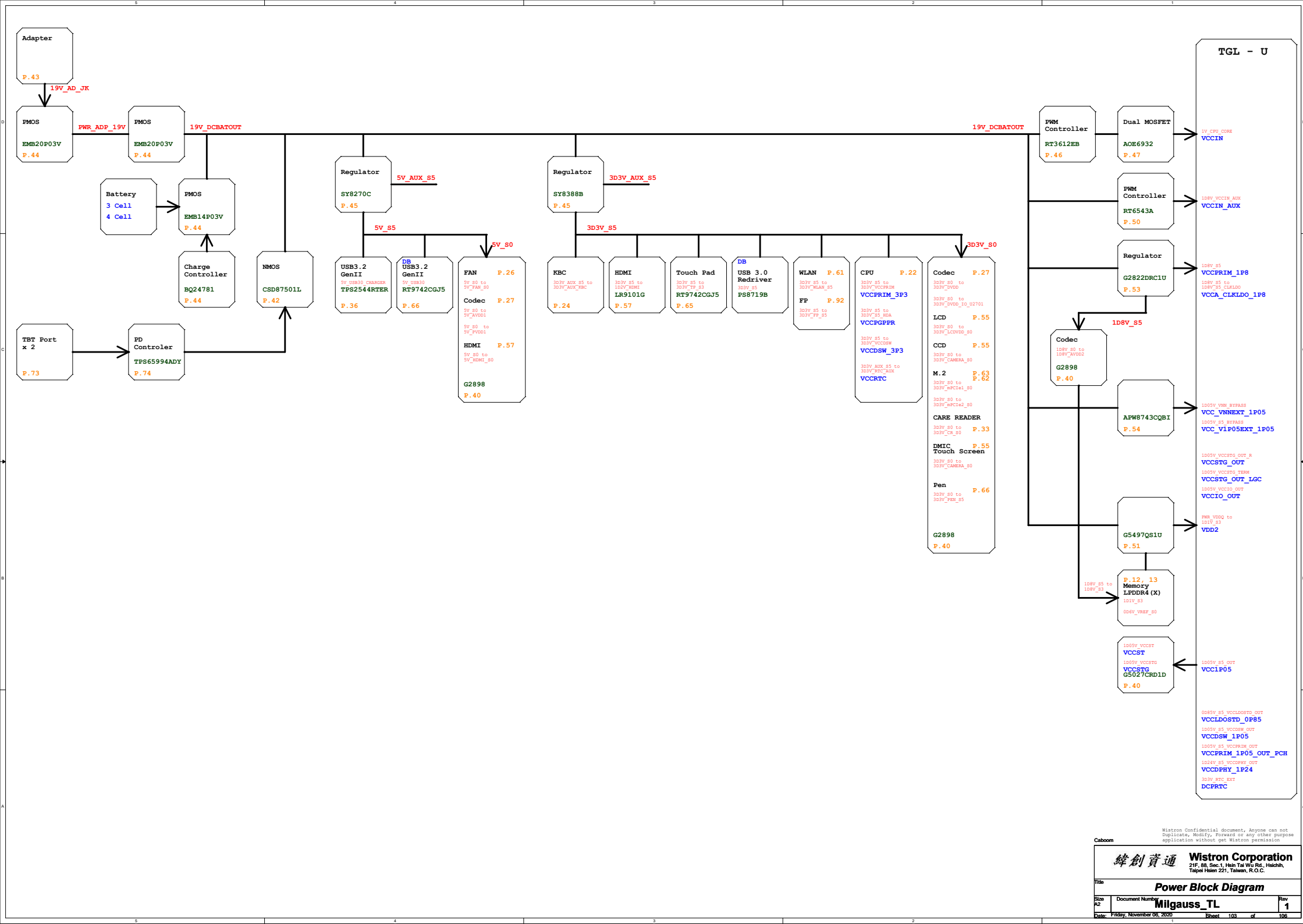
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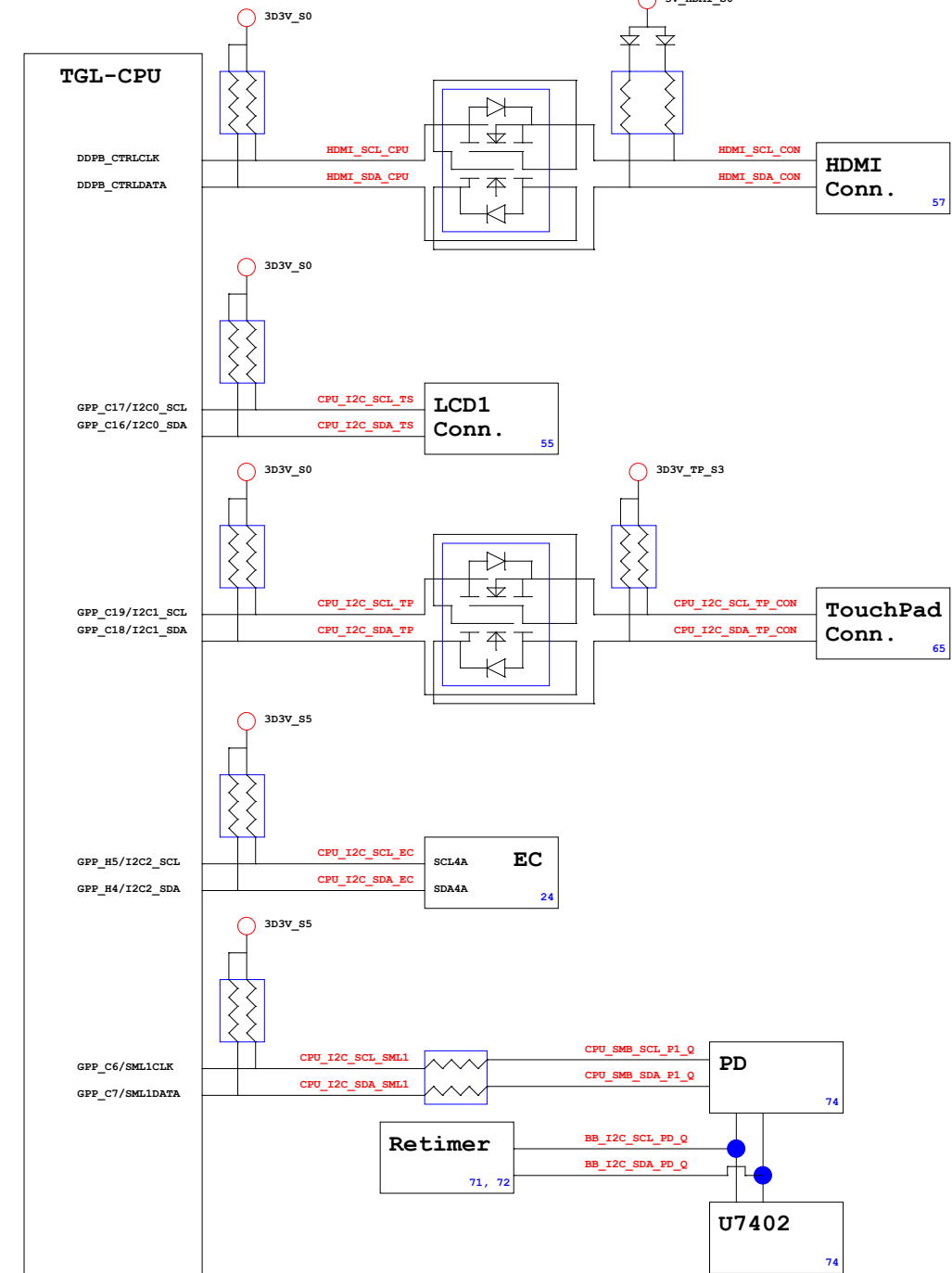
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Timing Diagram for G3 to S0[Non-Deep Sx Platform]

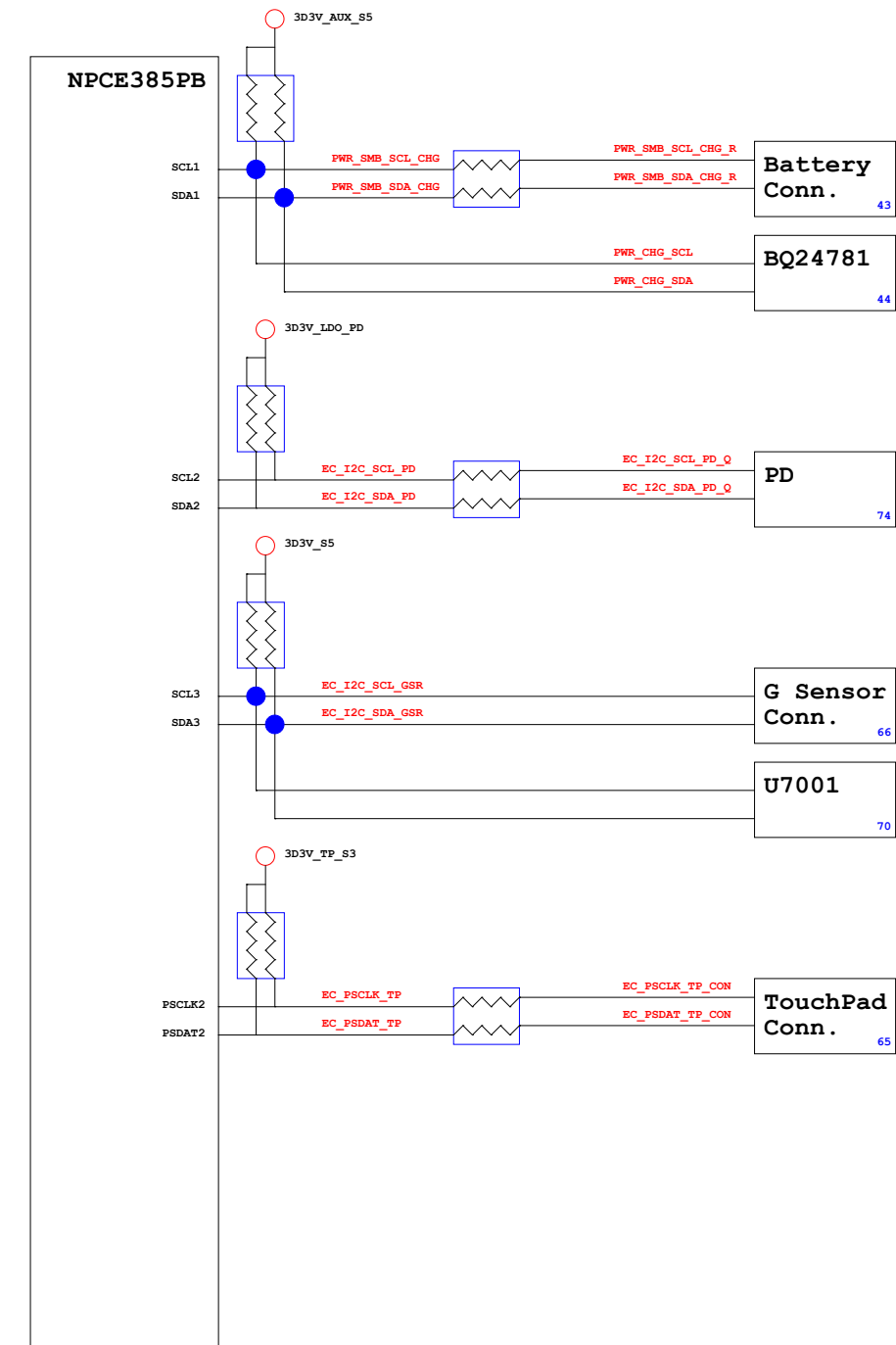




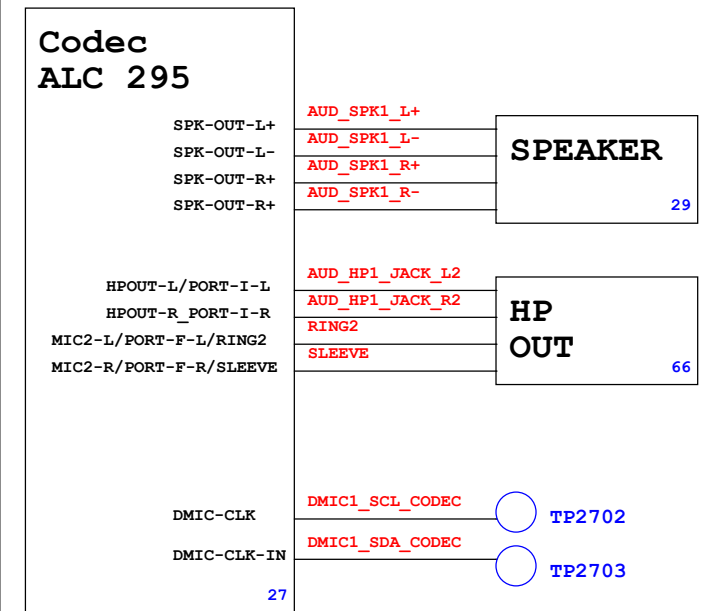
SOC SMBus/I2C Block Diagram



EC SMBus/I2C Block Diagram



Audio Block Diagram



Caboom

Title **THERMAL/AUDIO BLOCK DIAGRAM**

Size A3	Document Number Milgauss_TL	Rev 1
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32.768KHz

38.4MHz

WLAN1

SSD1

SSD2

XTL_32K_X1_CPU
XTL_32K_X2_CPU
XTL_38D4M_X1_CPU
XTL_38D4M_X2_CPU

WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N
CNV_WT_CLKP
CNV_WT_CLKN
CNV_WR_CLKP
CNV_WR_CLKN

SSD1_CLK_CPU_P
SSD1_CLK_CPU_N
SSD1_CLKREQ_CPU_N

SSD2_CLK_CPU_P
SSD2_CLK_CPU_N
SSD2_CLKREQ_CPU_N

RTCX1
RTCX2
XTAL_IN
XTAL_OUT

CLKOUT_PCIE_P1
CLKOUT_PCIE_N1
GPP_D6/SRCCLKREQ1#
CNVI_WT_CLKP
CNVI_WT_CLKN
CNVI_WR_CLKP
CNVI_WR_CLKN

CLKOUT_PCIE_P0
CLKOUT_PCIE_N0
GPP_D5/SRCCLKREQ0#

CLKOUT_PCIE_P2
CLKOUT_PCIE_N2
GPP_D7/SRCCLKREQ0#

Tiger Lake U

DDR0_CLK_N
DDR0_CLK_P
DDR1_CLK_N
DDR1_CLK_P
DDR0_CKE0
DDR0_CKE1
DDR1_CKE0
DDR1_CKE1

DDR2_CLK_N
DDR2_CLK_P
DDR3_CLK_N
DDR3_CLK_P
DDR2_CKE0
DDR2_CKE1
DDR3_CKE0
DDR3_CKE1

DDR4_CLK_N
DDR4_CLK_P
DDR5_CLK_N
DDR5_CLK_P
DDR4_CKE0
DDR4_CKE1
DDR5_CKE0
DDR5_CKE1

DDR6_CLK_N
DDR6_CLK_P
DDR7_CLK_N
DDR7_CLK_P
DDR6_CKE0
DDR6_CKE1
DDR7_CKE0
DDR7_CKE1

M_A_CLK_N0
M_A_CLK_P0
M_A_CLK_N1
M_A_CLK_P1
M_A_CKE0
M_A_CKE1
M_A_CKE2
M_A_CKE3

M_B_CLK_N0
M_B_CLK_P0
M_B_CLK_N1
M_B_CLK_P1
M_B_CKE0
M_B_CKE1
M_B_CKE2
M_B_CKE3

M_C_CLK_N0
M_C_CLK_P0
M_C_CLK_N1
M_C_CLK_P1
M_C_CKE0
M_C_CKE1
M_C_CKE2
M_C_CKE3

M_D_CLK_N0
M_D_CLK_P0
M_D_CLK_N1
M_D_CLK_P1
M_D_CKE0
M_D_CKE1
M_D_CKE2
M_D_CKE3

CK_C_B
CK_T_B
CK_C_A
CK_T_A
CKE0_B
CKE1_B
CKE0_A
CKE1_A

CK_C_B
CK_T_B
CK_C_A
CK_T_A
CKE0_B
CKE1_B
CKE0_A
CKE1_A

CK_C_B
CK_T_B
CK_C_A
CK_T_A
CKE0_B
CKE1_B
CKE0_A
CKE1_A

CK_C_B
CK_T_B
CK_C_A
CK_T_A
CKE0_B
CKE1_B
CKE0_A
CKE1_A

U7101
XTAL_25_IN
XTAL_25_OUT
BURNSIDE-BRIDGE

XTL_25M_X1_BB1
XTL_25M_X2_BB1

X7101
INPUT/OUTPUT#1
INPUT/OUTPUT#3

U7201
XTAL_25_IN
XTAL_25_OUT
BURNSIDE-BRIDGE

XTL_25M_X1_BB2
XTL_25M_X2_BB2

X7201
INPUT/OUTPUT#1
INPUT/OUTPUT#3